



DSIB

Data Storage and Interface Board

FEATURE HIGHLIGHTS

FOR HIGH-PERFORMANCE APPLICATIONS

The Data Storage and Interface Board (DSIB) is a daughterboard for the Xiphos Q8J processor designed to take advantage of the advanced capabilities and extensive I/O of the Q8J. The DSIB provides a large suite of high-speed and standard interfaces, as well as extensive mass memory storage to meet the needs of demanding applications that handle large amounts of data from multiple sources.

MASS DATA STORAGE

Offering two 1 TB SSD, the Q8J DSIB is equipped to store the large amounts of data that high-speed sensors generate. This SSD can store both pre and post-processed sensor data, which users can then downlink via radio interfaces, also available on the DSIB. The combination of high-performance processors and extensive FPGA fabric on the Q8J allows the onboard processing of sensor data, reducing demands on downlink bandwidth. Each SSD is individually powered and overcurrent protected to minimize power consumption while providing robustness and redundancy.

MULTIPLE GIGABIT ETHERNET PORTS

The Q8J DSIB provides 4 GigE interfaces, including magnetics, to connect to various external devices and sensors.

MULTIPLE SERIAL PORTS

The Q8J DSIB provides 7 RS-422 and 1 RS-485 serial ports for peripherals.

GENERIC LVDS I/Os

Finally, the Q8J DSIB also offers generic LVDS I/Os for a variety of interfaces that support your mission-specific needs. Typical implementations include SGMII (GigE over LVDS), custom LVDS, or multiple Spacewire interfaces using Xiphos' available IP core.

ADDITIONAL INTERFACES

The Q8J DSIB provides two CAN busses, one with redundant software-selectable inputs, and a PPS interface.

APPLICATIONS

The flexibility of the Q8J DSIB is ideal for:

- Serial and Ethernet payload hubs
- Payload data processors
- Payload bulk storage
- Network switching

PRODUCT INTEGRATION MODULE (PIM)

Each DSIB arrives with a detachable PIM to support development. This PIM provides standard commercial interfaces (e.g. JTAG, USB) and other lab development features.

SOFTWARE DEVELOPMENT

To support software development on Linux workstations, Xiphos provides an Application Development Kit with standard Linux libraries for C/C++. Users can easily port code previously developed for Linux desktop and server applications to the DSIB. DSIB hardware and logic interfaces are all accessible through standard Linux and Xilinx kernel drivers, or through custom drivers provided by Xiphos.

LOGIC DEVELOPMENT

Logic development uses standard Xilinx development tools. Xiphos, Xilinx and many third party vendors also offer a wide range of compatible reusable logic cores for Xilinx FPGAs.

FLIGHT HERITAGE

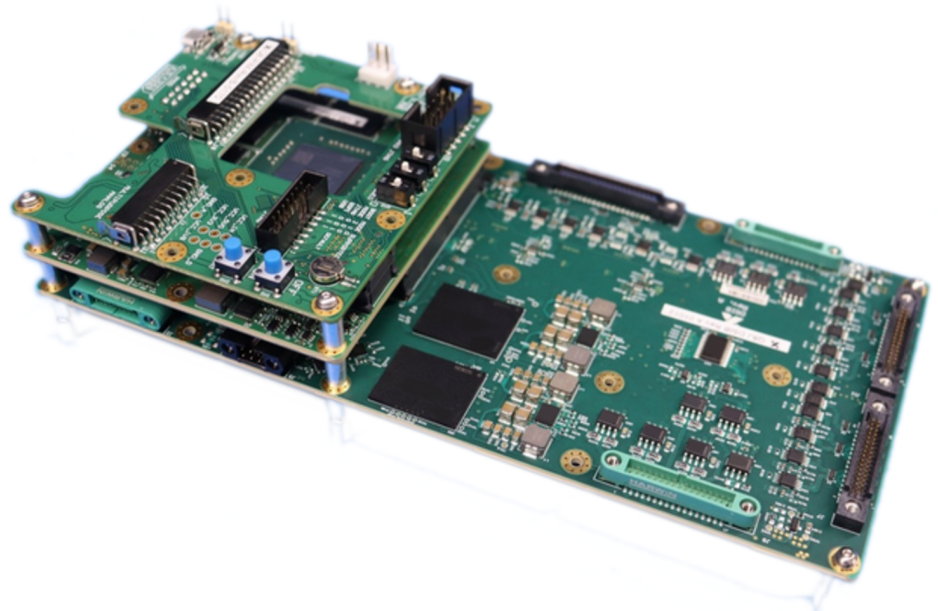
The Q8J processor of the DSIB was first deployed in space in 2023, with 13 total now on orbit. DSIB first launch is in 2025:



Other flight heritage products in the current Xiphos Q-Card family include the Q7S, Q8S, and Q8JS.



Over 200 Q-Cards have flown to date. Xiphos has been flying previous generations of the Xiphos Q-Card family since 2002.



CHARACTERISTICS

MASS STORAGE DEVICES

- 2 PCIe Gen 3 x4 interfaces
- Independent data and power control
- Overcurrent protected
- 1 TB capacity each (in TLC mode)

COMMUNICATION INTERFACES

- 4x GigE (1Gbps) ports with magnetics
- 2x CAN bus controllers
 - One controller capable of switching between two transceivers
- 7x RS422 ports, 1x RS485
- 1x RS422/RS485 (full or half-duplex, factory-configured)
- 16x LVDS outputs
- 12x LVDS inputs
- 4x factory-configured LVDS I/Os

OPERATING SYSTEM

- Yocto Linux BSP (LTS distribution)

FORM FACTOR

- 90 mm x 190 mm x 25 mm, 260 g (DSIB + Q8J) + mounting HW)

ENVIRONMENTAL

- Operating temperature: -40 to +60C

POWER

- Input voltage: 9 to 13V (12V nominal)
- 12W typical with all interfaces active and 1 SSD

Q8JS FLIGHT MODEL INCLUDES

- Triple mode redundancy in Control FPGA
- EDAC-protected RAM
- Upset and multi-current monitoring
- Overcurrent protection (multiple)
- FPGA bit-stream scrubbing
- Software robustness / watchdog
- 30krad TID lifetime

BLOCK DIAGRAM

