Sidekiq™ X4

RF Transceiver • High Performance

INTEGRATION MANUAL

V1.2 - MARCH 03, 2022

CHANGELOG

Revision	Date	Description	Author
0.1	2019-11-07	Pre-release draft, initial version	Barry L
0.2	2020-01-31		Barry L
0.3	2020-07-02	Updated figure 5, section 7.2	Barry L
1.0	2020-09-10	Updated figure 3 to reflect rev C architecture. Added data sheet link to the Si53307 clock mux. Markdown conversion	Barry L
1.1	2020-09-16	Added i2c device table, I/O exp and current sensor info, data sheet links, update integration steps	Barry L
1.2	2022-03-03	Added ad9528 initialization information	Barry L

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INTRODUCTION

This document is a detailed summary of the hardware interfaces for Epiq Solutions' Sidekiq X4 multichannel RF transceiver card [1], a VITA 57.1 compliant FPGA mezzanine card (FMC) utilizing the high pin count (HPC) interface. This manual is meant to be used in conjunction with the Sidekiq X4 Hardware Users' Manual [5] to provide a complete picture of the hardware signaling and interfacing requirements for Sidekiq X4. Those customers who do not wish to use the libsidekiq software API and FPGA reference design included in the Sidekiq X4 Platform Development Kit can use these two manuals to create their own FPGA firmware and software drivers from scratch.

It is strongly recommended to use Epiq's libsidekiq software and FPGA reference design. The Sidekiq X4 PDK includes both software and FPGA reference design code to control/interface with one of several different FPGA carrier cards with an FMC host interface. These platforms are considered "golden reference" platforms where functionality of the Sidekiq X4 card is guaranteed to work. Epiq makes no claim that Sidekiq X4 will work on every FMC host platform, as different FMC host platforms may behave differently. Verifcation and validation of Sidekiq X4 on a customer's host platform with their own software and/or FPGA design is solely the responsibility of the customer. Every Sidekiq X4 board shipped from Epiq is fully tested in a golden reference platform and guaranteed working at time of shipment.

All documentation and support for Sidekiq X4 is provided through Epiq Solutions' support website [2], which can be found at: https://www.epiqsolutions.com/support

Please note that it is necessary to register prior to accessing the relevant information for your purchase.

LEGAL CONSIDERATIONS

The Sidekiq X4 is distributed all over the world. Each country has its own laws governing reception and transmission of radio frequencies. Each user of Sidekiq X4 and associated software is solely responsible for insuring that it is used in a manner consistent with the laws of the jurisdiction in which it is used. Many countries, including the United States, prohibit the transmission and reception of certain frequency bands, or receiving certain transmissions without proper authorization. Again, the user is solely responsible for the user's own actions.

PROPER CARE AND HANDLING

Each Sidekiq X4 card is fully tested by Epiq Solutions before shipment, and is guaranteed functional at the time it is received by the customer, and ONLY AT THAT TIME. Improper use of the Sidekiq X4 card can cause it to become non-functional. In particular, a list of actions that may cause damage to the hardware include the following:

- Handling the unit without proper static precautions (ESD protection) when the housing is removed or opened up
- Inserting or removing Sidekiq X4 from a host system when power is applied to the host system
- Connecting a transmitter to the RX port without proper attenuation
- Executing custom software and/or an FPGA bitstream that was not developed according to guidelines

The above list is not comprehensive, and experience with the appropriate measures for handling electronic devices is required.

REFERENCES

1. Sidekiq X4 Product Page

   https://epiqsolutions.com/modules/sidekiq-x4
2. Epiq Solutions Support Page

   https://www.epiqsolutions.com/support
3. VITA website

   http://www.vita.com
4. Analog Devices' ADRV9009 Wideband Transceiver Product Page

   http://www.analog.com/en/products/adrv9009.html
5. Sidekiq X4 Hardware User's Manual

   https://epiqsolutions.com/downloads/sidekiq-x4/
6. Analog Devices' AD9528 Product Page

   https://www.analog.com/en/products/ad9528.html
7. Analog Devices' AD5660 Product Page

   https://www.analog.com/en/products/ad5660.html
8. Atlanta Micro AM3025A Product Page

   https://www.atlantamicro.com/products/filters/am3025a/
9. Silicon Labs Si53307 Product Page

   https://www.silabs.com/timing/buffers/any-format-clock-buffers/device.si53307-b-gm
10. Texas Instruments TS5A63157 Product Page

    https://www.ti.com/product/TS5A63157
11. Texas Instruments INA219 Product Page

    https://www.ti.com/product/INA219

TERMS AND DEFINITIONS

Term	Definition
A/D	Analog to Digital converter
D/A	Digital to Analog converter
dB	Decibel
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	ElectroStatic Discharge
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
Fs	Sample Rate
GPS	Global Positioning System
HPC	High Pin Count (a variant of the VITA 57.1 electrical interface)
I/Q	In-Phase / Quadrature Phase
I2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
KHz	Kilohertz
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LPC	Low Pin Count (a variant of the VITA 57.1 electrical interface)
MHz	Megahertz
ObsRx	Observation Receiver
PDK	Platform Development Kit
PPS	Pulse Per Second
RF	Radio Frequency
Rx	Receive
SDK	Software Development Kit
SDR	Software Defined Radio
SSMC	A smaller version of the SubMiniature type C RF connector
TCXO	Temperature Compensated Crystal Oscillator
Tx	Transmit
USB	Universal Serial Bus

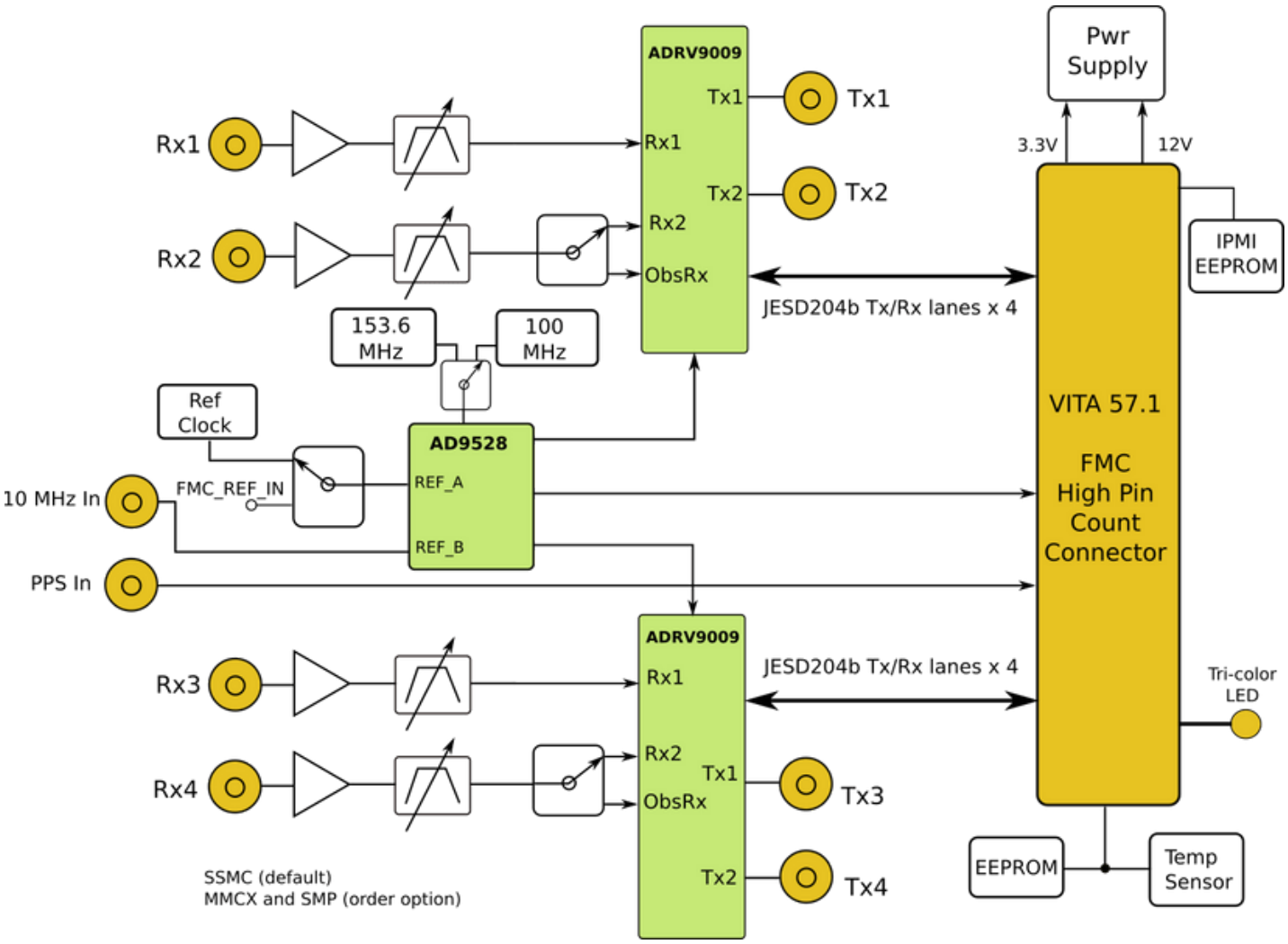
PLL	Phase Locked Loop
VITA	The standards body governing a variety of electro-mechanical specifications for computing systems (see [3] for details).

Table 1: *Terms and Definitions*

HARDWARE OVERVIEW

Sidekiq X4 is a high performance multi-channel RF transceiver card providing a complete “antenna-to-bits” solution in a VITA 57.1 FPGA mezzanine card (FMC) form factor. Sidekiq X4 leverages two Analog Devices' ADRV9009 wideband transceiver RFICs [4] to provide the core functionality of the card. The capability of the card is further enhanced with on-board circuitry to provide RF pre-select filtering on the RF receivers, support external synchronization inputs, and other features only found on Sidekiq X4. The key highlights of Sidekiq X4 are enumerated below:

- VITA 57.1 FMC compliant card providing a high pin count (HPC) interface
- RF tuning range from 1 MHz to 6 GHz
- Multiple modes of RX operation
  - Four phase coherent RX channels (200 MHz BW)
  - Dual independently tunable RX channels (up to 400 MHz BW)
- Multiple modes of TX operation
  - Four phase coherent TX channels (up to 400 MHz BW)
  - Dual independently tunable TX channels (up to 400 MHz BW)
- 16-bit A/D converters supporting sample rates up to 491.52 Msamples/sec
- 14-bit D/A converters supporting sample rates up to 491.52 Msamples/sec
- Seven-band RF pre-select filters on all RF receivers
- On-board 40 MHz TCXO reference clock (0.2 PPM stability)
- Accepts external 10 MHz clock reference and PPS inputs for synchronization
- Weight: 2.7 oz
- Power: 12 - 16 W typical (application dependent)
- Size: 84.1mm x 69mm



The remaining portion of this document is broken into three main sections:

- JESD Clocking System
- ADRV9009 RFIC Devices
- I2C Devices

JESD CLOCKING SYSTEM

The ADRV9009 uses the JESD204b high speed serial protocol to receive and transmit samples. For this reason, the AD9528 JESD clocking IC is used to drive both ADRV9009 devices as well as the host FPGA. Outputs 1 through 5 are routed to the FMC connector. Depending on routing to the FPGA host, any of these signals can be used as either DEV_CLK or SYSREF to satisfy JESD204b requirements.

There is also facility for driving the AD9528 reference from either the front panel J5, the on-board 40 MHz crystal or the FMC_REF_IN pins K4/K5 on the FMC connector.

Lastly, J6 can be configured as either the PPS input, SYSREF_IN or SYSREF_OUT (CLK9) to the AD9528.

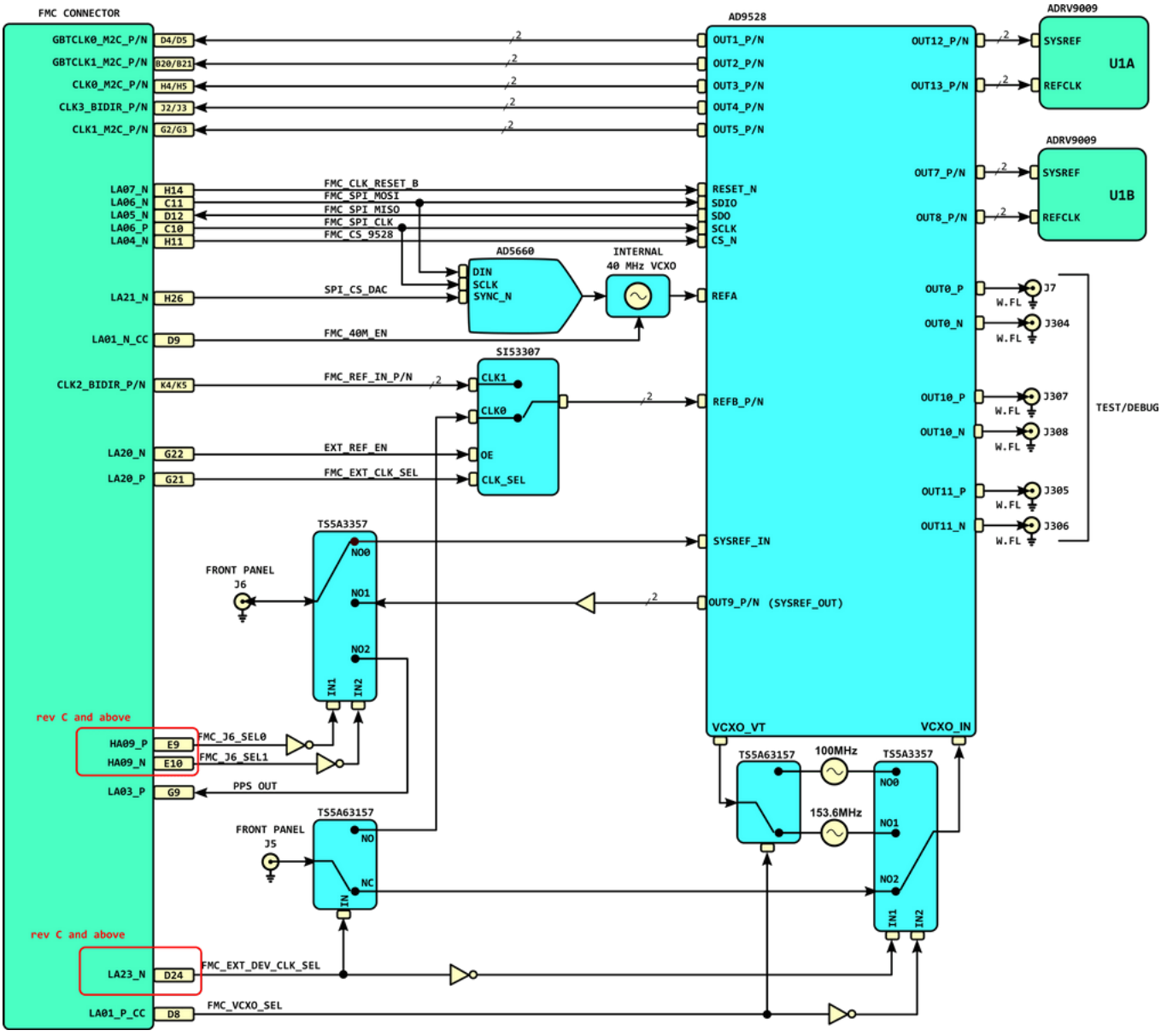


Figure 1: *NOTE: For rev B, see Appendix A*

REFERENCE SELECTION

The Sidekiq X4 clocking circuitry was designed to provide maximum flexibility for end users in terms of providing an external reference. The AD9528 can lock to any of 3 sources:

- On-board 40 MHz TCVXO (ASVTX12 from Abracon)
- Front panel J5
- Differential pair at the FMC connector

The Sidekiq X4 also provides a D/A for manually warping the on-board 40 MHz VCXO. This DAC is the Analog Devices AD5660 and is controlled over a SPI interface driven via the FMC interface. Refer to the data sheet for further information [7].

Reference Source	EXT_REF_EN	FMC_EXT_CLK_SEL	AD9528R Divider	FMC_40M_EN
On-board 40 MHz	0	X	A	1
External front panel (J5)	1	0	B	0
FMC pins (CLK2_BIDIR_P/N)	1	1	B	0

Table 2: *Reference Selection*

For voltage levels on these pins, refer to [5] (Sidekiq X4 Hardware User's Manual).

AD9528 CONFIGURATION

The AD9528 uses a dual-PLL architecture where the first PLL (PLL1) uses a very low loop bandwidth in order to mitigate noise on the incoming reference signal. PLL1 requires an external VCXO. The second PLL (PLL2) uses an internal VCXO.

VCXO Frequency	FMC_VCXO_SEL
100 MHz	0
153.6 MHz	1

Table 3: *VCXO_SEL truth table*

For voltage levels on these pins, refer to [5] (Sidekiq X4 Hardware User's Manual).

A range of different sample rates can be achieved with the AD9528 + VCXO selection. Since the output frequency of the AD9528 will determine the sample rate of the ADRV9009 devices, there are

two choices in VCXO frequencies which can be selected at run time—100 MHz or 153.6 MHz. The correct register settings for the dividers and charge pump current are dependent on the reference frequency provided. Below is a snippet of the schematic showing the loop filter values and the appropriate register settings give a 10 MHz reference signal.

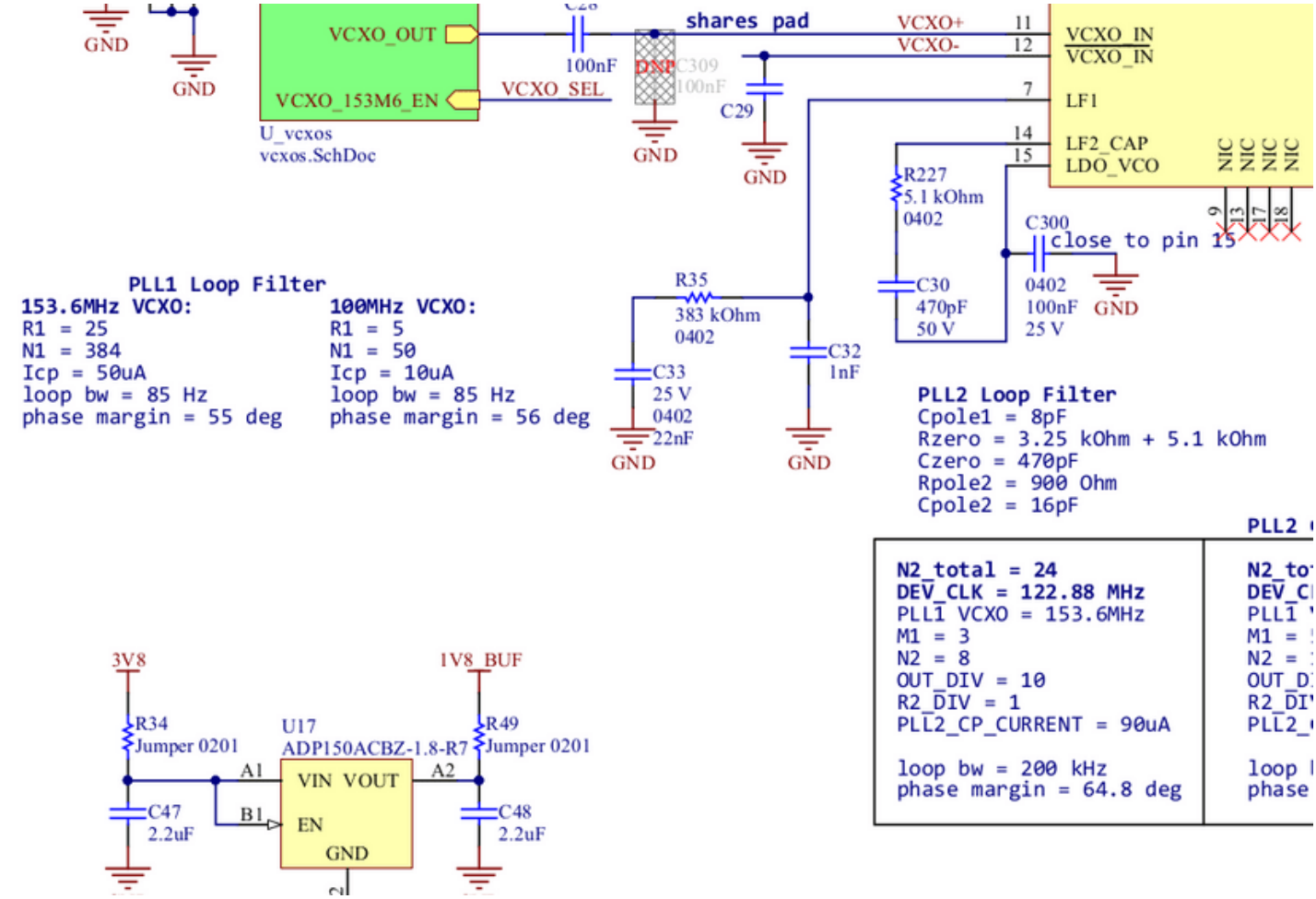


Figure 2: *AD9528 default configurations*

For debug purposes, the STATUS0 and STATUS1 signals are indicated by D4 and D5 respectively. The OUTPUT0 differential pair and SYSREF_IN differential pairs have also been routed to two W.FL connectors.

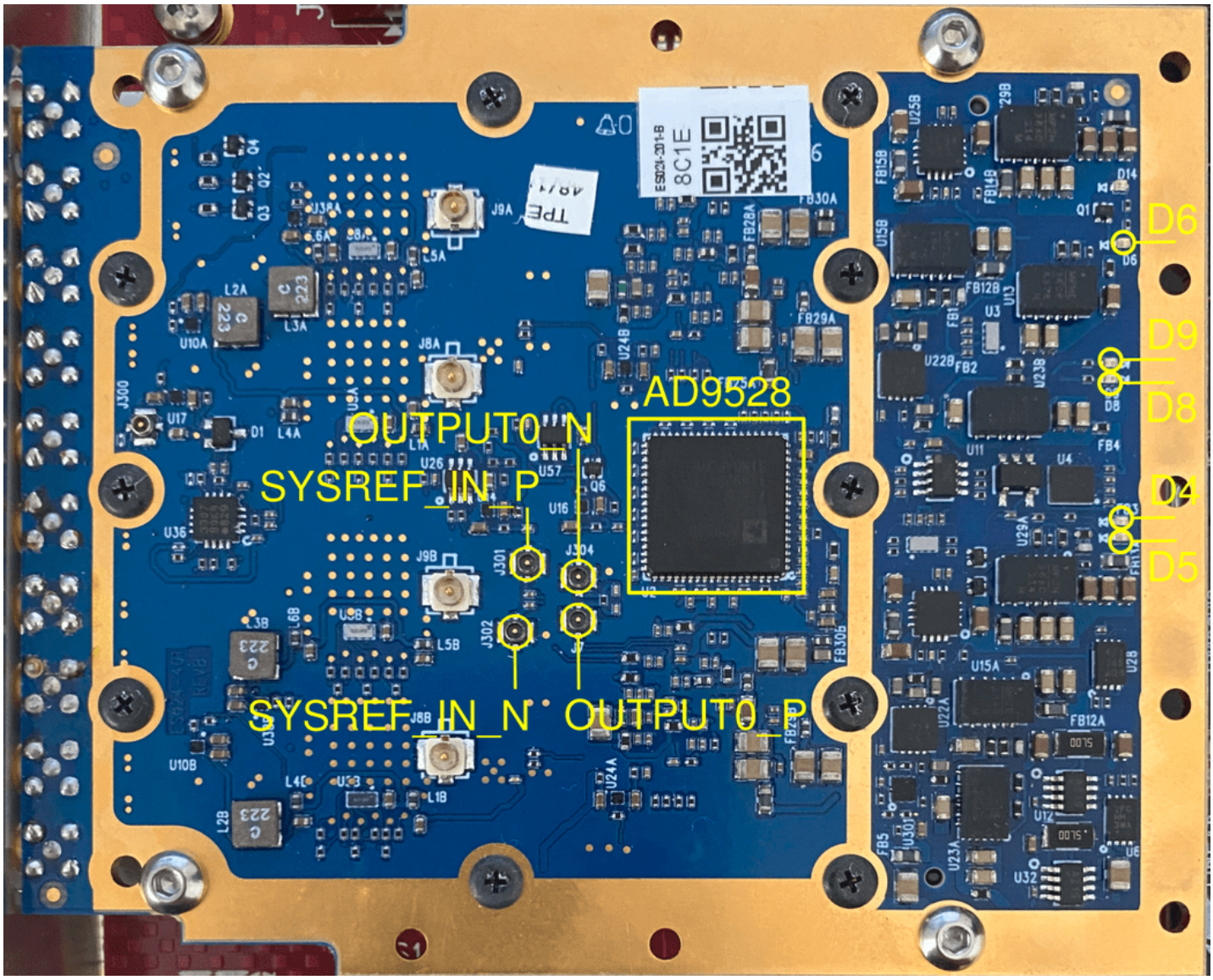


Figure 3: *AD9528 clock IC locations*

LED	Description
D4	STATUS0
D5	STATUS1
D6	3.3 VDC present
D8	153.6 MHz VCXO output enabled
D9	100 MHz VCXO output enabled

Table 4: *LEDs*

AD9528 REGISTER VALUES

The AD9528 register values to support a 122.88 Msps sample rate are listed in the table below. For more detailed information about the AD9528, refer to the Analog Devices data sheet[6].

- VCXO frequency needs to be set to 153.6 MHz

The output frequencies for the following clocks when operating at 122.88 MHz with the 40 MHz ref clock are listed below:

- OUT0,1,2,4,5,6,8,9,10,11,13 are at the DEVCLK frequency which happens to be the same as the sample clock frequency.
- OUT3 (FPGA SYSREF), OUT7 (RFIC B SYSREF), and OUT12 (RFIC A SYSREF) are SYSREF signals which only pulse a single time when the SPI requests a sysref signal.

ADDRESS	VALUE		ADDRESS	VALUE
0x0000	0x003c		0x030d	0x0000
0x0001	0x0080		0x030e	0x0009
0x0002	0x0000		0x030f	0x0000
0x0003	0x0005		0x0310	0x0080
0x0004	0x00ff		0x0311	0x0009
0x0005	0x0000		0x0312	0x0000
0x0006	0x0003		0x0313	0x0000
0x0007	0c005a		0x0314	0x0009
0x0008	0x0000		0x0315	0x0040
0x0009	0x0000		0x0316	0x0000
0x000a	0x0000		0x0317	0x0009
0x000b	0x0000		0x0318	0x0000
0x000c	0x0056		0x0319	0x0000
0x000d	0x0004		0x031a	0x0009
0x000e	0x0000		0x031b	0x0000
0x000f	0x0000		0x031c	0x0000
0x0100	0x0064		0x031d	0x0009
0x0101	0x0000		0x031e	0x0000
0x0102	0x0064		0x031f	0x0000
0x0103	0x0000		0x0320	0x0009
0x0104	0x0080		0x0321	0x0000
0x0105	0x0001		0x0322	0x0000
0x0106	0x0064		0x0323	0x0009
0x0107	0x0003		0x0324	0x0040
0x0108	0x0028		0x0325	0x0000

0x0109	0x0004		0x0326	0x0009
0x010a	0x0002		0x0327	0x0000
0x010b	0x0000		0x0328	0x0000
0x0200	0x001e		0x0329	0x0009
0x0201	0x0006		0x032a	0x0000
0x0202	0x0003		0x032b	0x0000
0x0203	0x0011		0x032c	0x0000
0x0204	0x0003		0x032d	0x0000
0x0205	0x0001		0x032e	0x0000
0x0206	0x0000		0x0400	0x0000
0x0207	0x0001		0x0401	0x0002
0x0208	0x0007		0x0402	0x0000
0x0209	0x0000		0x0403	0x0080
0x0300	0x0000		0x0404	0x0004
0x0301	0x0000		0x0500	0x0010
0x0302	0x0009		0x0501	0x0000
0x0303	0x0000		0x0502	0x0000
0x0304	0x0080		0x0503	0x00ff
0x0305	0x0009		0x0504	0x00ff
0x0306	0x0000		0x0505	0x0007
0x0307	0x0080		0x0506	0x0001
0x0308	0x0009		0x0507	0x000c
0x0309	0x0040		0x0508	0x00e7
0x030a	0x0000		0x0509	0x0000
0x030b	0x0009			
0x030c	0x0000			

Table 5: *AD9528 Register Values for 122.88 Msps Sample Rate*

ADRV9009 RFIC DEVICES

Configuration fo the ADRV9009 RFIC devices is handled through the SPI interface on the FMC. This SPI interface shares the same CLK, MOSI and MISO pins used for configuring the AD9528 JESD clock generator and the AD5660 D/A (previous section), with separate chip selects for each device. For specific details on how to configure the ADRV9009, refer to the Analog Devices' product page [4].

ADRV9009 CONNECTIONS TO FMC

Below is a top level block diagram of the connections between both ADRV9009 devices and the FMC connector. Refer to the Sidekiq X4 Hardware Users' Manual [5] for specific pin numbers on the FMC.

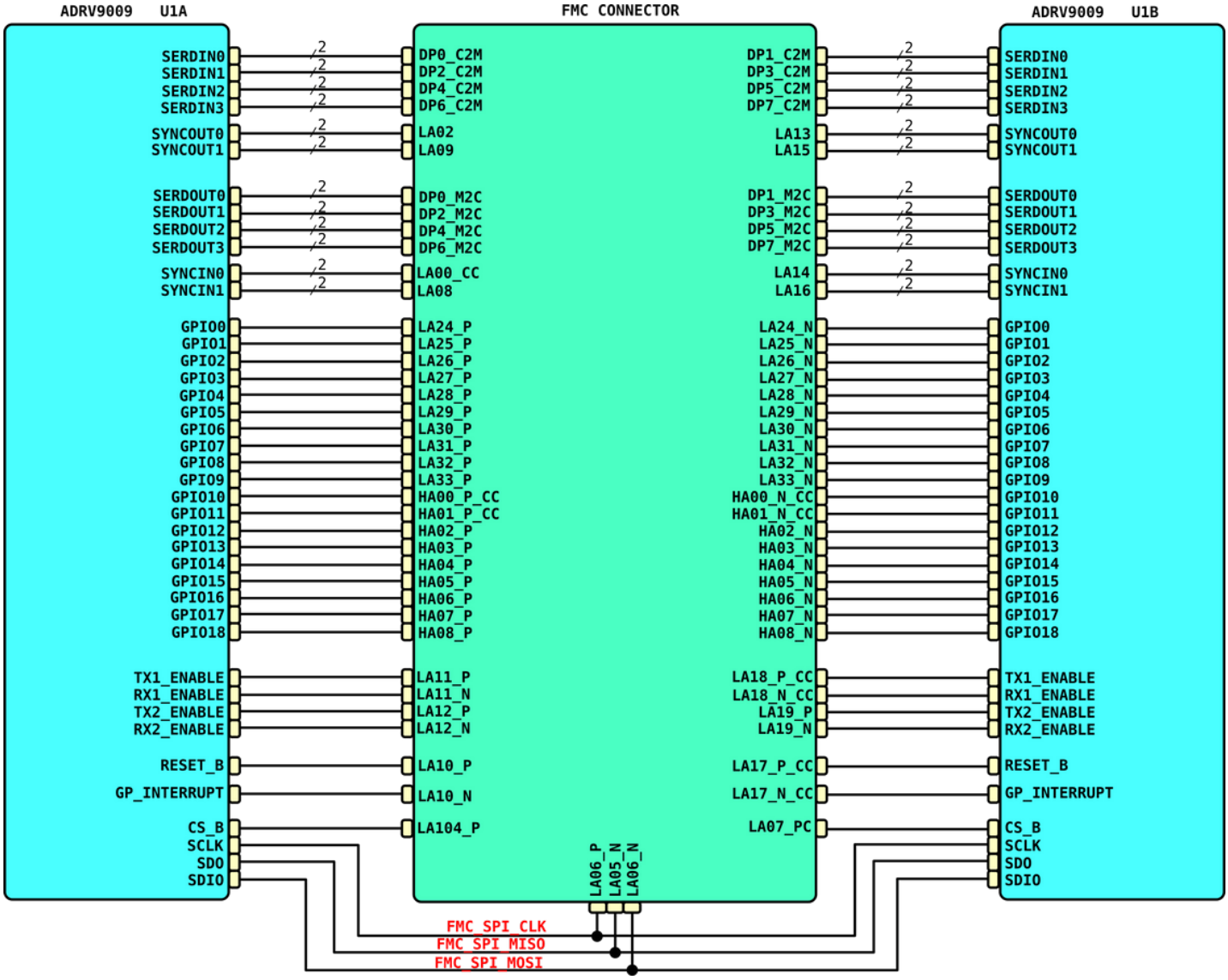


Figure 4: *FMC connections to ADRV9009 RFICs*

RF FRONT END

Below is a block diagram of the Sidekiq X4 RF front end for the transmit and receive paths. Both ADRV9009 RF front ends are identical.

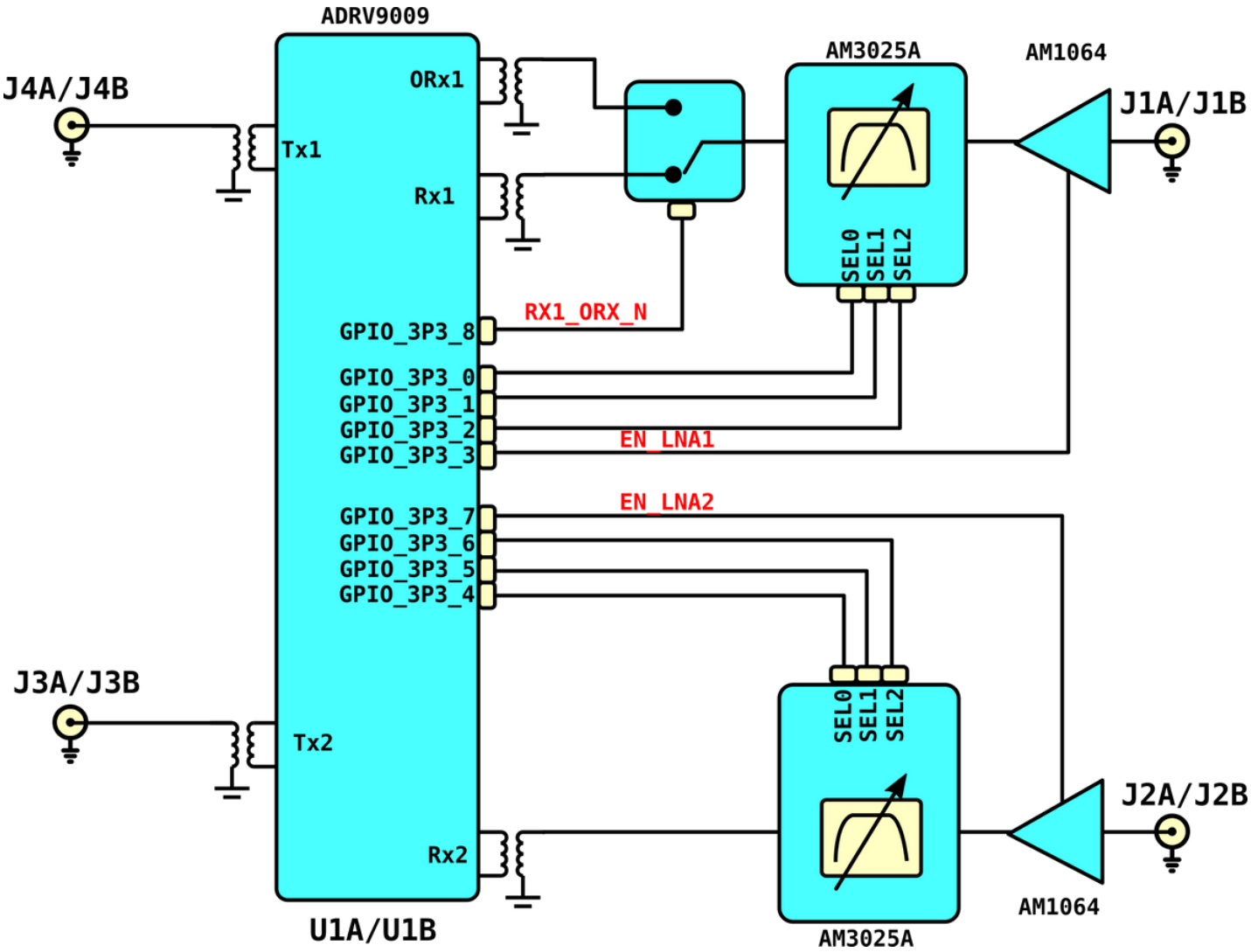


Figure 5: *RF Front End for both ADRV9009s*

The GPIO_3P3 signals from each ADRV9009 are used to control the state of the receive front end LNA and filter. These signals are controlled via SPI transactions to the ADRV9009. See [4] for details.

Connector	RFIC Port	RX1_ORX_N (state)
J1A	U1A – Rx1	1
J1A	U1A – ORx1	0
J2A	U1A – Rx2	don't care
J1B	U1B – Rx1	1

J1B	U1B – ORx1	0
J2B	U1B – Rx2	don’t care
J4A	U1A – Tx1	don’t care
J3A	U1A – Tx2	don’t care
J4B	U1B – Tx1	don’t care
J3B	U1B – Tx2	don’t care

Table 6: *Antenna port mapping*

The AM3025A is a 7 band switched bank filter from Atlanta Micro [8]. The truth table for the filter is below.

Band	**SEL[2:0]**	**Frequency Range (more or less)**
0 (bypass)	0x0	DC – 6 GHz
1	0x4	390 – 620 MHz
2	0x7	540 – 850 MHz
3	0x3	770 – 1210 MHz
4	0x2	1130 – 1760 MHz
5	0x5	1680 – 2580 MHz
6	0x1	2550 - 3880 MHz
7	0x6	3800 – 6000 MHz

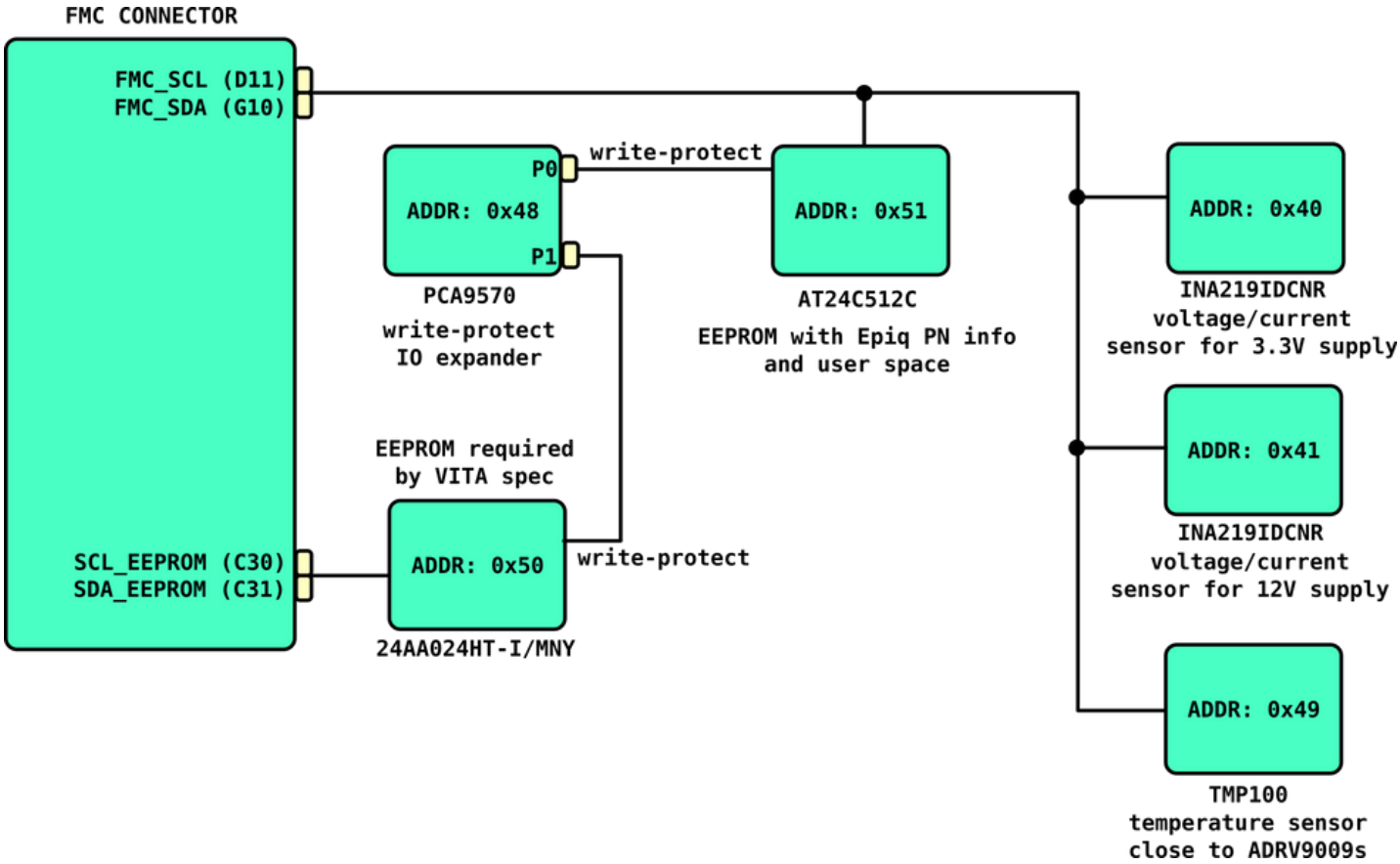
Table 7: *AM3025A truth table*

SIDEKIQ X4 I2C DEVICES

There are two separate I2C buses on the FMC connector. The VITA specification requires that there is a EEPROM. These I2C signals are at pins C30 (SCL) and C31 (SDA). See the VITA specification for further information [3].

The second bus is used to interface to several on-board devices which includes the following:

- Voltage/current sensors for +3.3V and +12V rails
- Temperature sensor
- EEPROM
  - contains Epiq part number, revision and serial number information
  - space for user storage
- IO expander used to write-protect VITA EEPROM and user EEPROM



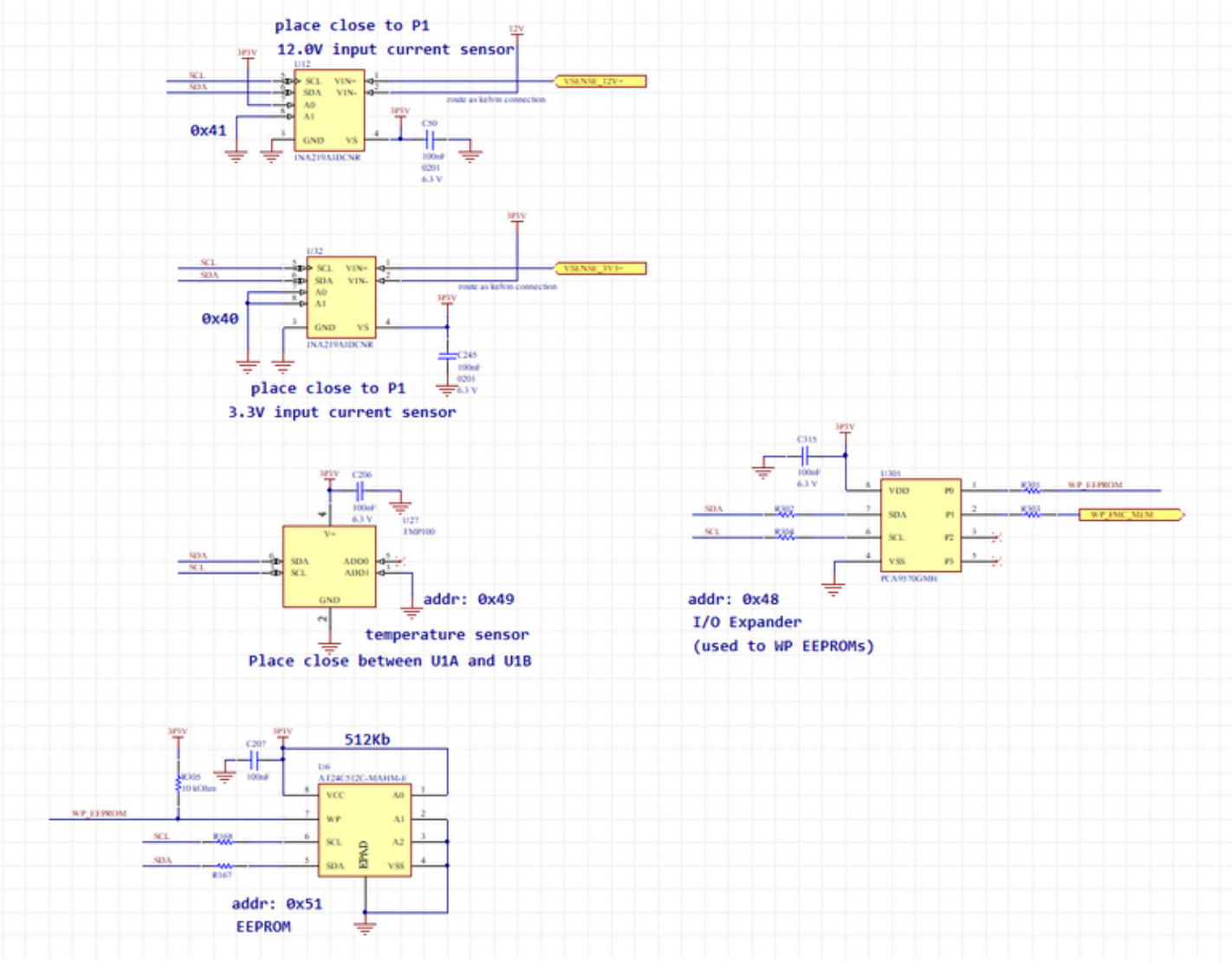


Figure 6: *Sidekiq X4 I2C devices*

Device	Address
TMP100 temp sensor	0x49
VITA EEPROM (2 Kbits)	0x50
User EEPROM (512 Kbits)	0x51
INA219 3.3V current Sensor	0x40
INA219 12V current Sensor	0x41
IO Expander (WP EEPROM)	0x48

Table 8: *I2C Device Addresses*

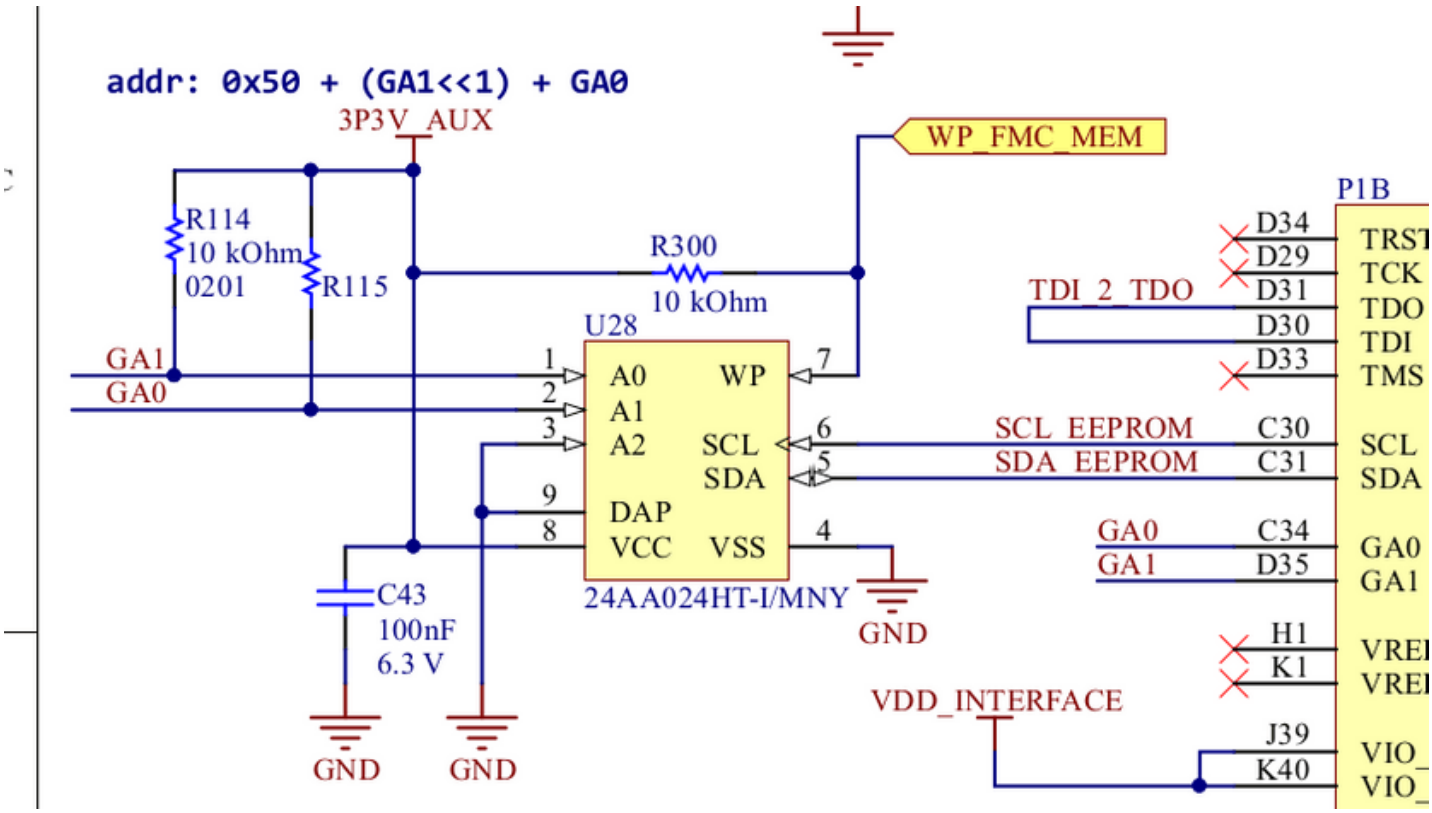
IO EXPANDER

The IO Expander (WP EEPROM), not pictured, is used for write-protection of both the FMC_EEPROM and the on-board Sidekiq EEPROM.
The write-protect signals are active-high. You will need to set the appropriate WP signal low if you wish to modify the memory.

CURRENT SENSORS 3.3V AND 12V

Please refer to the TI INA219 Product page [5] for additonal information on device usage such as calibration register and values.
Note, the VSENSE*12V+ shunt resistor & the VSENSE*3V3+ shunt resistor are 0.005 ohm.
Rohm P/N: PMR18EZPFU5L00 Current Sense Resistor - SMD 1206 0.005ohm 1% AEC-Q200

VITA EEPROM



VITA EEPROM ADDRESS MAP

TBD

USER EEPROM ADDRESS MAP

TBD

OTHERS

FRONT PANEL 1PPS

The front panel 1PPS input connector (J6) goes to a dual output buffer. One side of the buffer drives the PPS LED (D14), the other side goes directly to the FMC_PPS pin on the FMC connector (G9).

LED CONTROL

There is a tri-color LED which is visible through the front panel. A logic high on any of the LED pins will turn on the respective color. See truth table below.

FMC PIN	LED color
G24	Red
G25	Green
D23	Blue

Table 9: *LED pins*

FMC POWER REQUIREMENTS

The Sidekiq X4 is compliant with the VITA 57.4 specification. Therefore, the VITA specification should be the guiding document when designing the host power supply for the Sidekiq X4. There are no special sequencing requirements for the power supplies. The power sequencing is handled on the Sidekiq X4.

INTEGRATION STEPS

The following is a suggested path for integrating Sidekiq X4 into a customer’s platform.

1. Get board powered up to verify LEDs and current draw through I2C current monitor as expected.
    - The 1.8V **VADJ** supply is provided by the host and should be verified on the host side. if you can communicate to the I2C devices, then VADJ will be present/functioning.
    - Reasonable current draw for Sidekiq X4 after the devices have been initialized where the clock chip (AD9528) has been configured along with the two RFICs (ADRV9009) are in the range of 500 mA on the +12V supply and around 900 mA on the +3.3V supply.
      Current draw before initialization will most likely be lower.
2. Verify EEPROM access
3. Bring up AD9528 JESD clock IC to verify you can generate 122.88 MHz sample clock
4. Bring up a single ADRV9009, verifying you can program its firmware, get JESD lock, etc all using the ADI API
5. Bring up the RF front end
6. Verify RX signal on all antenna ports at different frequencies
7. Verify TX signal on all antenna ports at different frequencies
8. Verify external PPS and 10MHz functions as expected

APPENDIX A – REV B JESD CLOCKING STRUCTURE

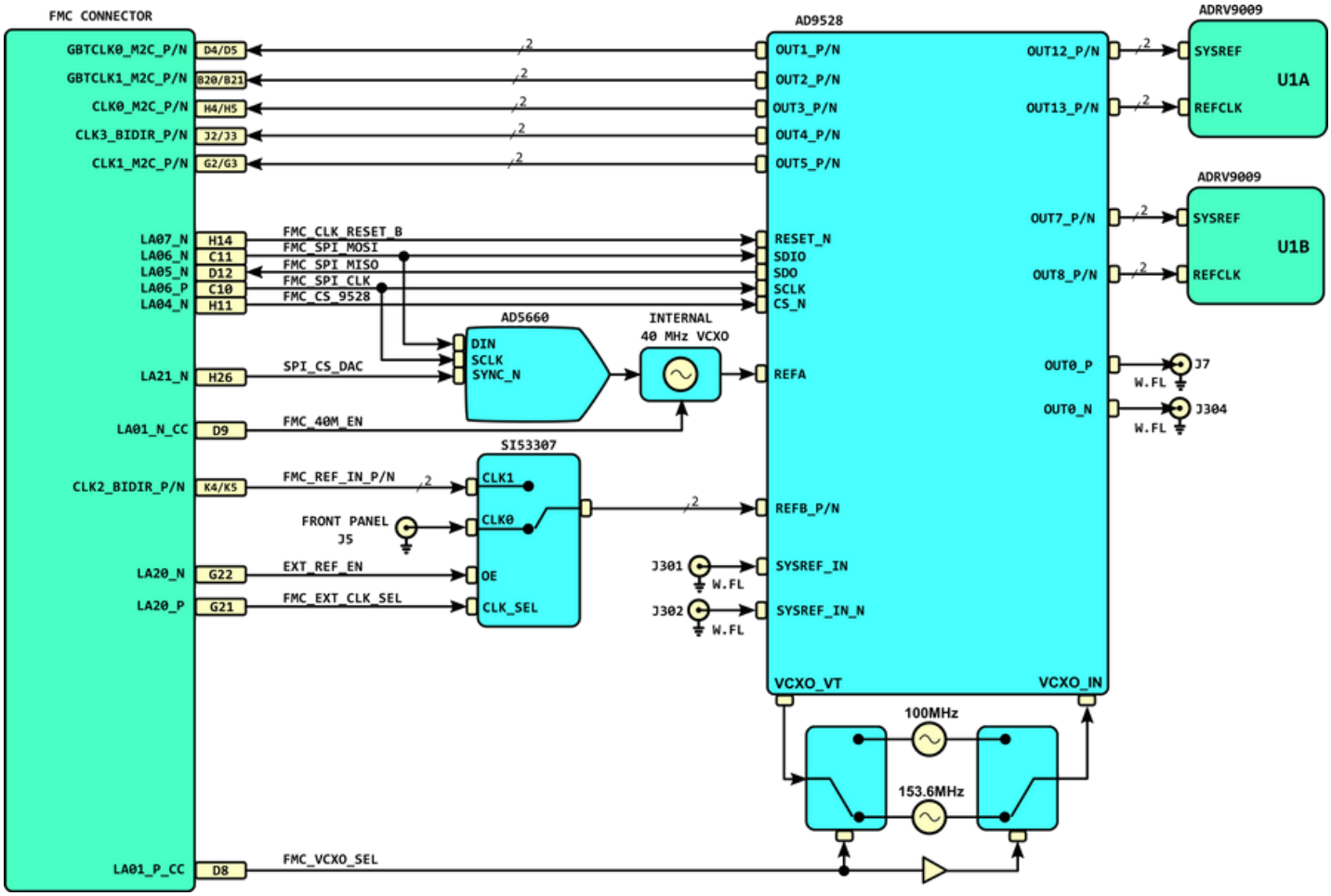


Figure 7: *Sidekiq X4 rev B JESD Clocking Structure*