Sidekiq™ X4

RF Transceiver • High Performance

HARDWARE USER MANUAL

V1.4 - APRIL 07, 2022

CHANGELOG

Revision	Date	Description	Author
0.1	2018-10-06	Pre-release draft, initial version	Barry L
0.2	2018-10-13	Update diagrams, pictures	Barry L
0.3	2019-01-03	Updated section 7, figure 4, section 8	Barry L
0.4	2019-04-25	Updated section 9, FMC pinout	Barry L
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0.6	2019-07-31	Updated Appendix A	Barry L
0.7	2019-08-06	Additional updates to Appendix A	Barry L
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1.1	2020-06-29	Converted to Markdown, table updates	Barry L
1.2	2020-09-21	LPC pin & description corrections, added TDD info	Barry L
1.3	2021-09-02	Update MTBF format and transmit attenuation range	Barry L
1.4	2022-04-07	Update tcvcxo info and added Rx pre-select filter band table	Barry L

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INTRODUCTION

This document provides an overview and usage details of Epiq Solutions' Sidekiq X4 multichannel RF transceiver card [1], a VITA 57.1 compliant FPGA mezzanine card (FMC) utilizing the high pin count (HPC) interface. Sidekiq X4 provides the entire “antenna-to-bits” high performance RF signal chain in a single card, allowing a customer to radically shorten their typical RF platform development cycle. Sidekiq X4 can interface to any FMC HPC host system, where an FPGA and additional follow on processing would be executed. Epiq Solutions provides an FPGA reference design as well as software drivers, libraries, and test applications to demonstrate the usage of Sidekiq X4 interfaced to a COTS FMC host platform with a PCIe interface to a host computing system. This reference design, as well as the software drivers, libraries, and test applications, can then be ported to other FMC host carrier systems for custom deployment scenarios.

The following topics will be discussed:

- Overview of the Sidekiq X4 hardware interfaces
- Sidekiq X4 usage/integration options
- Sidekiq X4 example usage in the FMC host platform reference design

All documentation and support for Sidekiq X4 is provided through Epiq Solutions' support website which can be found at: https://www.epiqsolutions.com/support

Please note that it is necessary to register prior to accessing the relevant information for your purchase.

LEGAL CONSIDERATIONS

The Sidekiq X4 is distributed all over the world. Each country has its own laws governing reception and transmission of radio frequencies. Each user of Sidekiq X4 and associated software is solely responsible for insuring that it is used in a manner consistent with the laws of the jurisdiction in which it is used. Many countries, including the United States, prohibit the transmission and reception of certain frequency bands, or receiving certain transmissions without proper authorization. Again, the user is solely responsible for the user's own actions.

PROPER CARE AND HANDLING

Each Sidekiq X4 card is fully tested by Epiq Solutions before shipment, and is guaranteed functional at the time it is received by the customer, and ONLY AT THAT TIME. Improper use of the Sidekiq X4 card can cause it to become non-functional. In particular, a list of actions that may cause damage to the hardware include the following:

- Handling the unit without proper static precautions (ESD protection) when the housing is removed or opened up
- Inserting or removing Sidekiq X4 from a host system when power is applied to the host system
- Connecting a transmitter to the RX port without proper attenuation
- Executing custom software and/or an FPGA bitstream that was not developed according to guidelines

The above list is not comprehensive, and experience with the appropriate measures for handling electronic devices is required.

REFERENCES

1. Sidekiq X4 Product Page

   https://epiqsolutions.com/modules/sidekiq-x4
2. Epiq Solutions Support Page

   https://www.epiqsolutions.com/support
3. VITA website

   http://www.vita.com
4. Analog Devices' ADRV9009 Wideband Transceiver Product Page

   http://www.analog.com/en/products/adrv9009.html
5. Hi Tech Global's Product Page for the HTG-K800 FPGA PCIe Carrier Card

   http://www.hitechglobal.com/Boards/Kintex-UltraScale.htm
6. Berquist Thermal Gap Pad Material

   http://www.bergquistcompany.com/thermal_materials/gap-pad.htm

TERMS AND DEFINITIONS

Term	Definition
A/D	Analog to Digital converter
D/A	Digital to Analog converter
dB	Decibel
ESD	ElectroStatic Discharge
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
Fs	Sample Rate
GPS	Global Positioning System
HPC	High Pin Count (a variant of the VITA 57.1 electrical interface)
I/Q	In-Phase / Quadrature Phase
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LFM	Linear Feet per Minute
LNA	Low Noise Amplifier
LPC	Low Pin Count (a variant of the VITA 57.1 electrical interface)
MHz	Megahertz
MMCX	Micro-Miniature Coaxial RF Connector
ObsRx	Observation Receiver
PC	Personal Computer
PDK	Platform Development Kit
PPS	Pulse Per Second
RF	Radio Frequency
Rx	Receive
SDK	Software Development Kit
SDR	Software Defined Radio
SMP	Sub-Miniature push-on RF connector
SSMC	A smaller version of the SubMiniature type C RF connector
TCVCXO	Temperature Compensated Voltage Controlled Crystal Oscillator

TDD	Time Division Duplex
Tx	Transmit
USB	Universal Serial Bus
Vih	Voltage Input High (the minimum logic level high voltage)
VITA	The standards body governing a variety of electro-mechanical specifications for computing systems (see [3] for details).

Table 1: *Terms and Definitions*

HARDWARE OVERVIEW

Sidekiq X4 is a high performance multi-channel RF transceiver card providing a complete “antenna-to-bits” solution in a VITA 57.1 FPGA mezzanine card (FMC) form factor. Sidekiq X4 leverages two Analog Devices' ADRV9009 wideband transceiver RFICs [4] to provide the core functionality of the card. The capability of the card is further enhanced with on-board circuitry to extend the RF tuning range, provide RF pre-select filtering on the RF receivers, support external synchronization inputs, and other features only found on Sidekiq X4.

The key highlights of Sidekiq X4 are enumerated below:

- VITA 57.1 FMC compliant card providing a high pin count (HPC) interface
- RF tuning range from 75 MHz to 6 GHz, able to capture 1 MHz to 6 GHz
- Four phase coherent RF receivers with common LO
- Two independently tunable RF receivers
- Four phase coherent RF transmitters with common LO
- Supports RF channel bandwidths up to 400 MHz
- 16-bit A/D converters supporting sample rates up to 491.52 Msamples/sec
- 14-bit D/A converters supporting sample rates up to 491.52 Msamples/sec
- Seven-band RF pre-select filters on all RF receivers
- On-board 40 MHz TCVCXO reference clock (+/- 1 PPM stability)
- Accepts external 10 or 40 MHz clock reference and PPS inputs for synchronization
- Weight: 2.7 oz
- Power: 6 - 12 W typical (application dependent)
- Size: 84.1mm x 69mm

Figure 1: *Sidekiq X4*

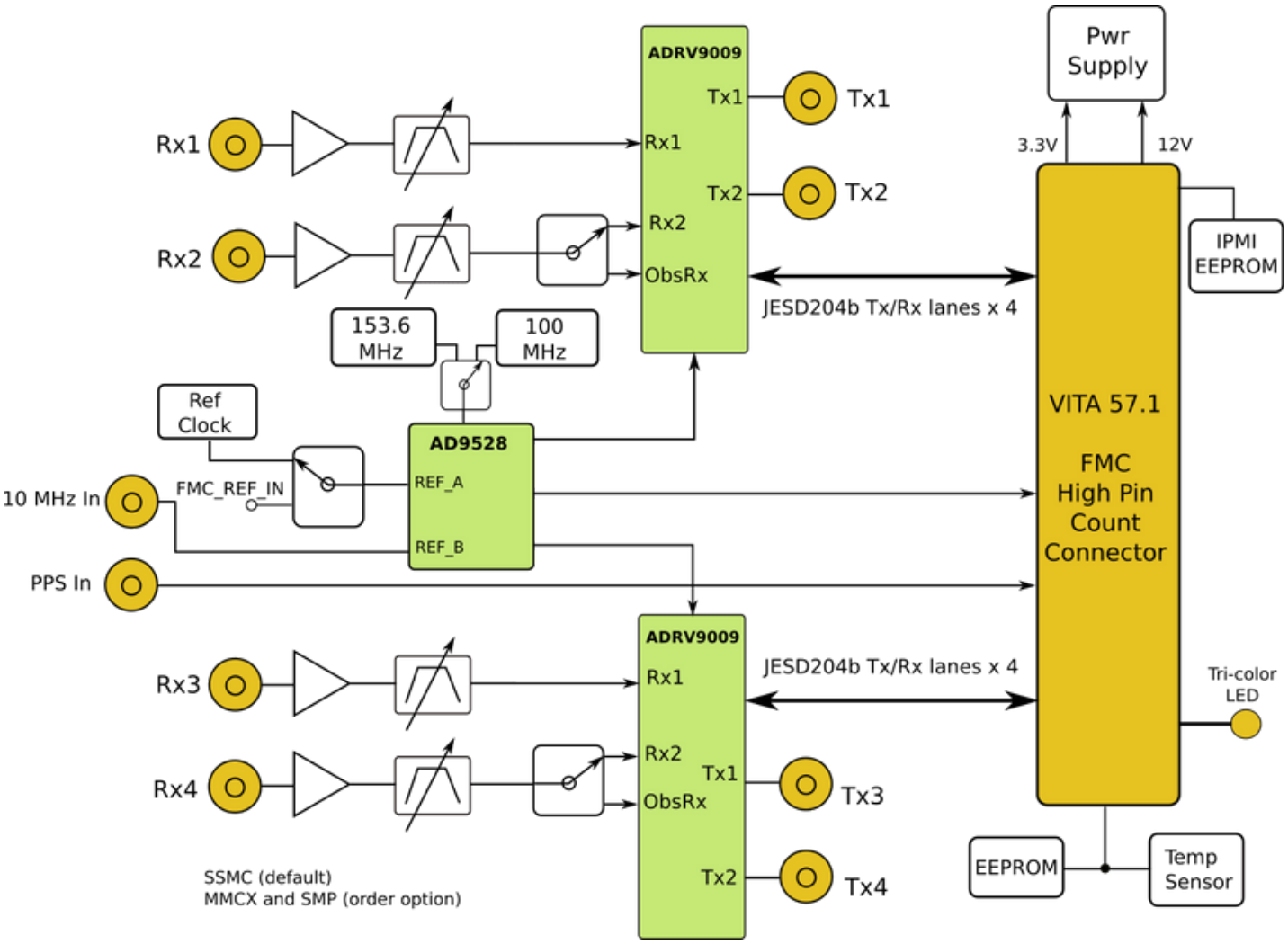

Figure 2: *Block diagram of Sidekiq X4*

Note:

Sidekiq X4 is based on two TDD RFICs which means that Rx and Tx cannot be streaming at the same time when using just one RFIC. You can however, stream TX for an A* handle (RFIC A) simultaneously to receiving on a B* handle (RFIC B). Additionally, the LO frequency is shared across Rx and Tx frequencies. Specifically, skiq_rx_hdl_A1 / skiq_rx_hdl_A2 share the LO frequency with skiq_tx_hdl_A1 / skiq_tx_hdl_A2 and skiq_rx_hdl_B1 / skiq_rx_hdl_B2 share the LO frequency with skiq_tx_hdl_B1 / skiq_tx_hdl_B2 for the Sidekiq X4 product.

HARDWARE SPECIFICATION

RF RECEIVER SPECIFICATION (RX1, RX2, OBSRX)

RF Input	MMCX, 50 ohms (SMP and SSMC options)
Architecture	Zero-IF (direct conversion)
Tuning Range	75 MHz to 6 GHz, able to capture 1 MHz to 6 GHz
Tuning Step Size	2.3 Hz
Tuning Time	Refer to Sidekiq Software Development Manual, Release 4.13.x or later - Methods of LO frequency tuning
Tuning Time in Fast Frequency Hopping mode	Refer to Sidekiq Software Development Manual, Release 4.13.x or later - Methods of LO frequency tuning
Typical Noise Figure	6-8 dB below 3 GHz, 8-10 dB above 3 GHz
Spurious-Free Dynamic Range	75 – 80 dB typical
Typical IIP3 (at 8 dB noise figure)	+8 dBm
Gain Control Range	0 to 30 dB (Rx1 and Rx2); 0-18 dB (ObsRx);1 dB steps
Gain Control Modes	Manual or AGC
A/D Converter Sample Rate	Up to 491.52 Msamples/sec
A/D Converter Sample Width	16 bits
Typical I/Q Balance	70 dB
A/D JESD204b Lane Rate	Up to 12.288 Gbps
# of JESD204b Lanes Utilized	RxA1, RxA2, RxB1, RxB2: 1 lane ObsRxA, ObsRxB: 1 or 2 lanes (Fs dependant)
Max RF input signal (without damage)	+27 dBm
RF full scale input (at max gain)	-20 dBm (frequency dependent)
RF Pre-Select Filter Passbands	Automatically selected when tuning the RF receiver; see Figure 3 for passband details

Table 2: *rx specification*

RF TRANSMITTER SPECIFICATION (TX1, TX2)

RF Output	MMCX, 50 ohms (SMP and SSMC options)
Architecture	Zero-IF (direct conversion)
Tuning Range	75 MHz to 6 GHz, able to output 1 MHz to 6 GHz
Tuning Step Size	2.3 Hz
Tuning Time	Refer to Sidekiq Software Development Manual, Release 4.13.x or later - Methods of LO frequency tuning
Tuning Time in Fast Frequency Hopping mode	Refer to Sidekiq Software Development Manual, Release 4.13.x or later - Methods of LO frequency tuning
Gain Control Range	0 to 41.75 dB, 0.25 dB steps
Max RF Transmit Output Power	5 dBm to 0 dBm (<3 GHz)-10 dBm to -5 dBm (>3 GHz)
Typical OIP3	+26 dBm
D/A Converter Sample Rate	Up to 491.52 Msamples/sec
D/A Converter Sample Width	14 bits
Typical I/Q Balance	> 60 dB
D/A JESD204b Lane Rate	Up to 12.288 Gbps
# of JESD204b Lanes Utilized	1 or 2 lanes (sample rate dependent)

Table 3: *tx specification*

CLOCK/SYNCHRONIZATION SPECIFICATION

Port	MMCX, 50 ohms (SMP and SSMC options)
On Board Reference Clock	40 MHz TCVCXO (+/- 1 PPM stability) P/N: Abracon ASVTX-12-C-40_000MHZ-H10-T
External Reference Clock Input Frequency	10 or 40 MHz
External Reference Clock Input Power Range	-5 dBm to +10 dBm
On Board VCXO for DEV_CLK	Software switchable between two options (both populated on board):Option 1: 153.6 MHz (PN: Bliley BCVCB153M6) Option 2: 100 MHz (PN: Bliley BCVCB100)
PPS Input Level	Vadj logic level (1.8V or 2.5V), 5V tolerant

Table 4: *clock/sync specification*

HARDWARE SPECIFICATION

Component Temperature Rating	-40 deg C to +85 deg C
FMC Interface Type	High Pin Count
FMC Card Dimensions	84.1mm x 69mm
FMC Stacking Height	8.5mm
Weight	2.7 oz
Temperature Sensor	-55 deg C to +125 deg C (+/- 2 deg C resolution)(P/N: Texas Instruments TMP100NA/250)
FMC (12P0V)	+12V
FMC (P3V3)	+3.3V
FMC Vadj Support	+1.8V / +2.5V

Table 5: *hardware specification*

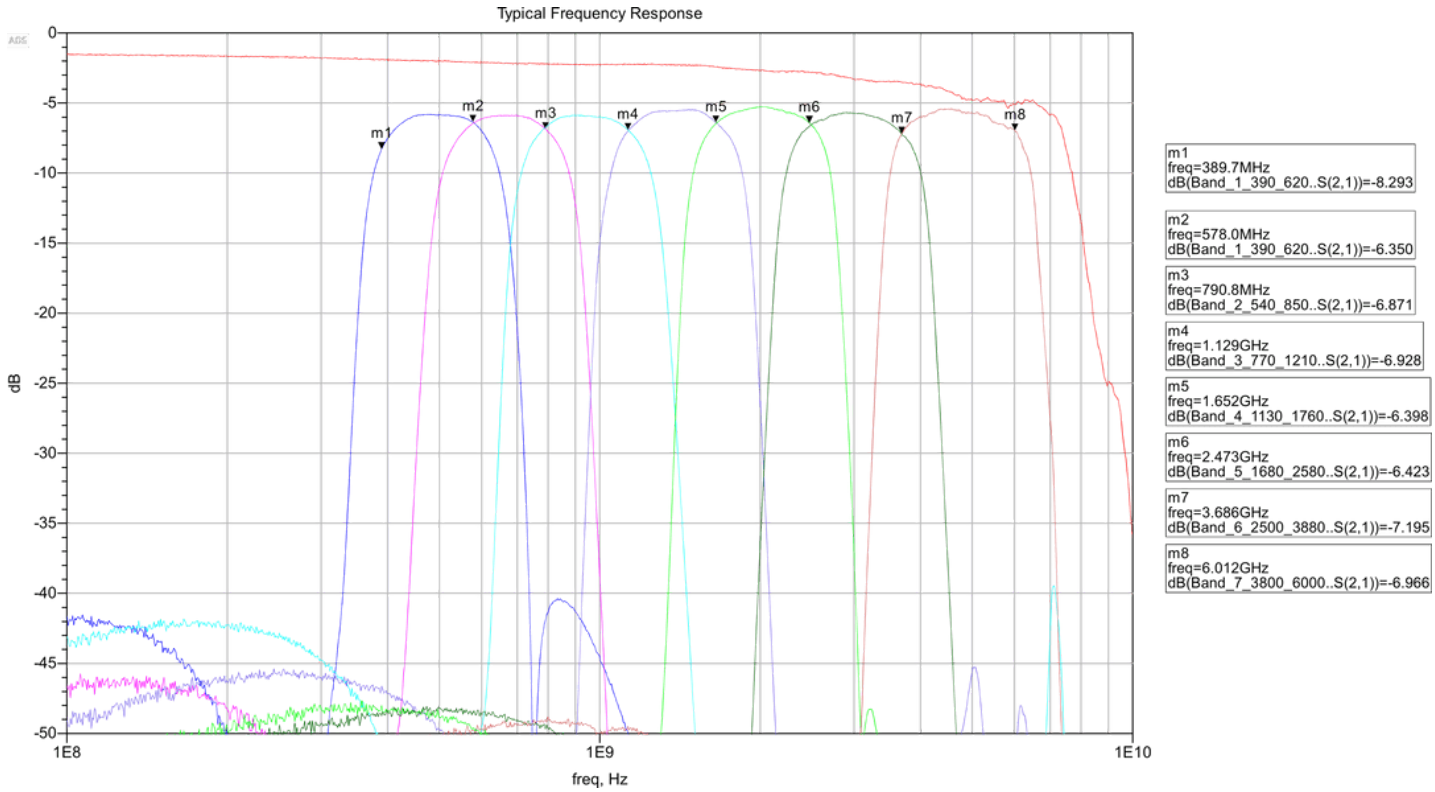

Figure 3: *Rx pre-select filter passband plot (filtering used on all receive channels)*

Filter Band	LO Tune Range
0 to 6000 MHz	<= 450 MHz
390 to 620 MHz	> 450 and <= 600 MHz
540 to 850 MHz	> 600 and <= 800 MHz
770 to 1210 MHz	> 800 and <= 1200 MHz
1130 to 1760 MHz	> 1200 and <= 1700 MHz
1680 to 2580 MHz	> 1700 and <= 2700 MHz
2500 to 3880 MHz	> 2700 and <= 3600 MHz
3800 to 6000 MHz	> 3600 and <= 6000 MHz

Table 6: *Rx pre-select filter bands*

HARDWARE INTERFACES

Sidekiq X4 provides is a standard VITA 57.1 compliant FMC card, and thus has a specific set of externally accessible hardware interfaces that are available to a user when the card is integrated into a system. Each of these hardware interfaces are enumerated in Figure 4, and are defined below.

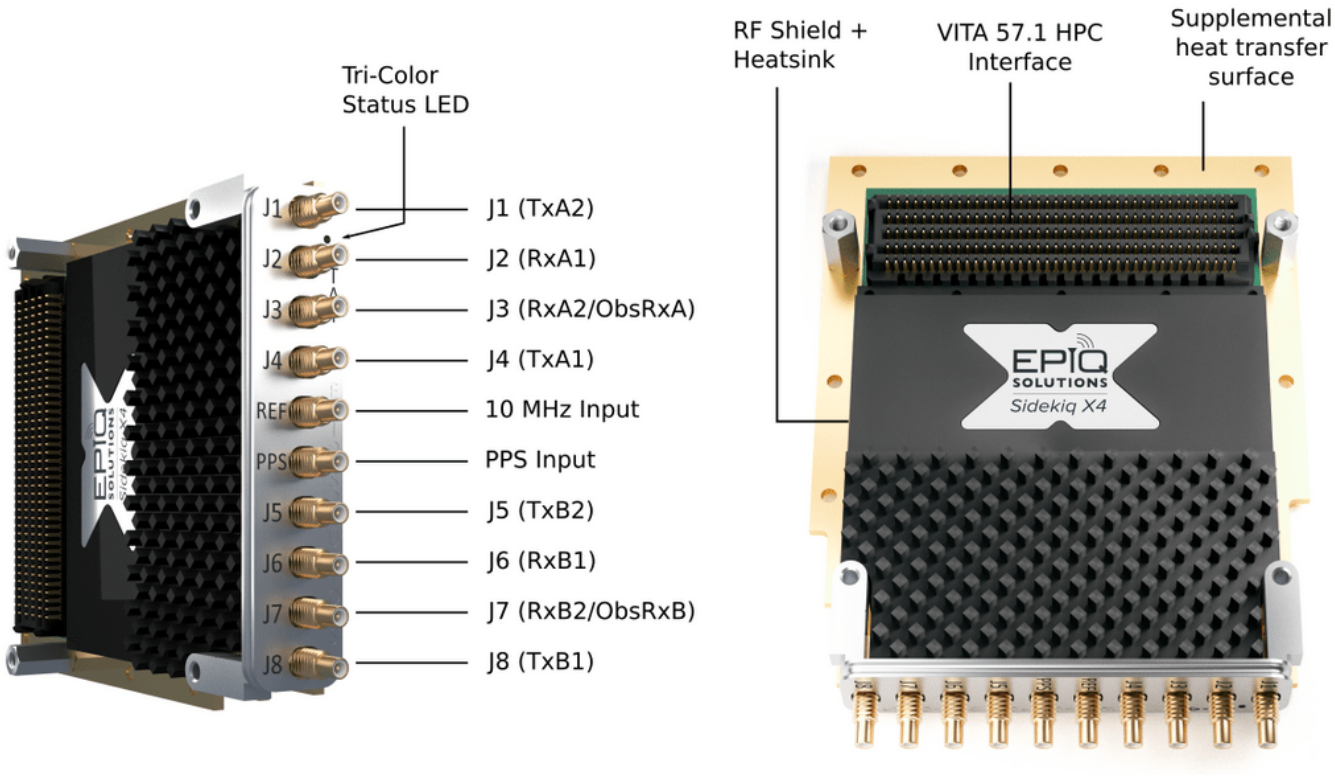

Figure 4: *Sidekiq X4 User Accessible I/O*

TRI-COLOR STATUS LED

The Tri-Color Status LED is a triple LED capable of emitting red, green, and blue light through the front panel light pipe. This LED is controlled through three GPIO signals (one for each color) accessible through the VITA 57.1 electrical interface. By default, this LED illuminates blue to indicate the card is powered up.

J1 (TXA2)

The J1 (TxA2) interface is an MMCX jack connector that provides an RF output path for the TxA2 antenna port. This antenna port is capable of transmitting signals between 1 MHz and 6 GHz, and shares a common LO with J4 (TxA1) and is phase synchronized to J8 (TxB1) and J5 (TxB2). The impedance of this port is 50 ohms.

J2 (RXA1)

The J2 (RxA1) interface is an MMCX jack connector that provides an RF input path for the RxA1 antenna port. This antenna port is capable of receiving signals between 1 MHz and 6 GHz. The RF receiver associated with this antenna port shares a common LO with J3 (RxA2) and is also phase coherent with J6 (RxB1) and J7 (RxB2).

J3 (RXA2/OBSRXA)

The J3 (RxA2) interface is an MMCX jack connector that provides an RF input path for the RxA2 antenna port. This antenna port is capable of receiving signals between 1 MHz and 6 GHz. The RF receiver associated with this antenna port shares a common LO with J2 (RxA1) and is also phase coherent with J6 (RxB1) and J7 (RxB2). Alternatively, this port can be configured as an Observation Rx port which can achieve sample rates up to 500 MSPS. The impedance of this port is 50 ohms.

J4 (TXA1)

The J4 (TxA1) interface is an MMCX jack connector that provides an RF output path for the TxA1 antenna port. This antenna port is capable of transmitting signals between 1 MHz and 6 GHz, and shares a common LO with J1 (TxA2) and is phase synchronized to J8 (TxB1) and J5 (TxB2). The impedance of this port is 50 ohms.

REF INPUT

The REF Input port is an MMCX jack connector that accepts an external 10 or 40 MHz input signal for the purpose of phase locking the on board reference clock. The acceptable signal level for this external input is between -5 dBm and +10 dBm. By default, Sidekiq X4 has a 40 MHz reference clock on board that is used for phase locking the system. In order to use an external reference input, the libsidekiq software API provides a function call to disable on the on-board 40 MHz reference and lock on to this external 10 or 40 MHz reference input. *Revision C of Sidekiq X4 can also use this port (configured via libsidekiq) as either the REF Input (default) or the input for an externally-provided DEV_CLK which is required for multi-card synchronization.*

PPS INPUT

The PPS Input port is an MMCX jack connector that accepts a pulse per second (PPS) input signal for the purpose of providing a temporal frame of reference relative to this PPS edge. This PPS signal is routed through a SN74LVC2G17YZPR buffer directly to the FMC electrical interface, and thus routes directly into the FPGA on the host system. The PPS edge is expected to be a rising edge with a fast slew rate, with a logic level high defined as any voltage between 0.85V and 5V, dependent on Vadj (+1.8V / +2.5V). This PPS signal is used by the Sidekiq X4 FPGA reference design to latch the digital timestamp of when the PPS edge occurs in the FPGA, and can then be queried by the libsidekiq software API. It is also possible to coordinate other actions to take place based on the occurrence of a PPS edge, such as starting Rx or Tx streaming. *Revision C of Sidekiq X4 can also use this port (configured via libsidekiq) as either the PPS input (default), SYSREF_IN or SYSREF_OUT to/from the AD9528 for multi-card synchronization.*

J5 (TXB2)

The J5 (TxB2) interface is an MMCX jack connector that provides an RF output path for the TxB2 antenna port. This antenna port is capable of transmitting signals between 1 MHz and 6 GHz, and shares a common LO with J8 (TxB1) and is phase synchronized to J4 (TxA1) and J1 (TxA2). The impedance of this port is 50 ohms.

J6 (RXB1)

The J6 (RxB1) interface is an MMCX jack connector that provides an RF input path for the RxB1 antenna port. This antenna port is capable of receiving signals between 1 MHz and 6 GHz. The RF receiver associated with this antenna port shares a common LO with J7 (RxB2) and is also phase coherent with J2 (RxA1) and J3 (RxA2).

J7 (RXB2/OBSRXB)

The J7 (RxB2) interface is an MMCX jack connector that provides an RF input path for the RxB2 antenna port. This antenna port is capable of receiving signals between 1 MHz and 6 GHz. The RF receiver associated with this antenna port shares a common LO with J6 (RxB1) and is also phase coherent with J2 (RxA1) and J3 (RxA2). Alternatively, this port can be configured as an Observation Rx port which can achieve sample rates up to 500 MSPS. The impedance of this port is 50 ohms.

J8 (TXB1)

The J8 (TxB1) interface is an MMCX jack connector that provides an RF output path for the TxB1 antenna port. This antenna port is capable of transmitting signals between 1 MHz and 6 GHz, and shares a common LO with J5 (TxB2) and is phase synchronized to J4 (TxA1) and J1 (TxA2). The impedance of this port is 50 ohms.

> **Note:** for conduction cooled applications, MMCX or SMP connectors are available. Contact Epiq Solutions for details.

RF SHIELD & HEATSINK

The RF shield/heatsink provides both RF isolation from spurious RF signals, while also providing a thermal dissipation path for the card when used in convection cooled application. A minimum air flow of TBD LFM is required to ensure that the heat generated by the card is adequately dissipated.

VITA 57.1 HPC CONNECTOR

The VITA 57.1 HPC connector is the primary electrical interface for connecting Sidekiq X4 to a host system. The complete pin mapping for signals accessible through this HPC interface on Sidekiq X4 is defined in the FMC High Pin Count (HPC) Section.

> Note: It is assumed that the standard Sidekiq X4 FPGA reference design + libsidekiq software API is being utilized by the host system. This reference design + software API provides all of the infrastructure and control necessary to control the operation of the card, as well as stream data between the card and the host system. The Sidekiq X4 FPGA reference design + libsidekiq software API can be ported to alternate host platforms other than the PDK reference platform. Please contact Epiq Solutions for details.

SUPPLEMENTAL HEAT TRANSFER SURFACE

The Supplemental Heat Transfer Surface provides an additional thermal relief surface for the FMC card. This area surrounding the edge of the card is defined in the VITA 57.1 specification for the purpose of thermal relief, and can be used in conduction cooled deployments. For convection cooled deployments with the appropriate airflow moving over the RF shield & heatsink, this supplemental heat transfer surface is unused.

FMC PIN MAP

The following table provides the definition of all of the pins utilized on the FMC interface of Sidekiq X4. This includes pins allocated to both the low pin count (LPC) portion of the connector, as well as the high pin count (HPC) portion of the connector. Additional details of the FMC electrical interface can be found in the VITA 57.1 specification [3].

> Note: the definition and allocation of these pins typically have a specific meaning in the context of both the FMC specification, and more importantly, the Sidekiq X4 FPGA reference design delivered with the Sidekiq X4 PDK. Epiq Solutions provides support for Sidekiq X4 when used in conjunction with the Sidekiq X4 FPGA reference design and associated libsidekiq software library.

FMC LOW PIN COUNT (LPC) SECTION

FMC Signal Name	FMC Pin	Sidekiq X4 Net Name	Description	Logic/Standard	Type	Comments
DP0_C2M_P	C2	DP0_C2M.DP	JESD input lane for TX SERDIN0 on RFIC A	CML (current mode logic)	input	
DP0_C2M_N	C3	DP0_C2M.DN	JESD input lane for TX SERDIN0 on RFIC A	CML (current mode logic)	input	
DP0_M2C_P	C6	DP0_M2C.DP	JESD output lane for RX SERDOUT0 on RFIC A	CML (current mode logic)	output	
DP0_M2C_N	C7	DP0_M2C.DN	JESD output lane for RX SERDOUT0 on RFIC A	CML (current mode logic)	output	
LA06_P	C10	FMC_SPI_CLK	SPI clock	VADJ	input	
LA06_N	C11	FMC_SPI_MOSI	SPI data in	VADJ	input	
LA10_P	C14	RESETB_A	reset for RFIC A (active low)	VADJ	input	
LA10_N	C15	GP_INTERRUPT_A	interrupt from RFIC A	VADJ	input	
LA14_P	C18	SYNCIN0_B.D_P	JESD RX channel sync for RFIC B	LVDS	input	
LA14_N	C19	SYNCIN0_B.D_N	JESD RX channel sync for RFIC B	LVDS	input	
LA18_P_CC	C22	TX1_ENABLE_B	enables TX channel 1 for RFIC B	VADJ	input	
LA18_N_CC	C23	RX1_ENABLE_B	enables RX channel 1 for RFIC B	VADJ	input	
LA27_P	C26	GPIOA3	GPIO bus to RFIC A	VADJ	input/ output	

LA27_N	C27	GPIOB3	GPIO bus to RFIC B	VADJ	input/ output	
SCL	C30	SCL_EEPROM	FMC EEPROM I2C clock	3.3V	input	
SDA	C31	SDA_EEPROM	FMC EEPROM I2C data	3.3V	input/ output	
GA0	C34	GA0	geographical address 1 for EEPROM (intentionally opposite)	3.3V	input	
12P0V	C35	VSENSE_12V+	main 12V supply input	12V	DC in	main 12V supply
12P0V	C37	VSENSE_12V+	main 12V supply input	12V	DC in	main 12V supply
3P3V	C39	VSENSE_3V3+	main 3.3V supply input	3.3V	DC in	main 3.3V supply
PG_C2M	D1	PG_C2M	power good host to mezzanine	3.3V	input	
GBTCLK0_M2C_P	D4	GBTCLK0_M2C.DP	FPGA global clock from SKIQ clock IC port 1	LVDS	output	
GBTCLK0_M2C_N	D5	GBTCLK0_M2C.DN	FPGA global clock from SKIQ clock IC port 1	LVDS	output	
LA01_P_CC	D8	FMC_VCXO_SEL	selects VCXO. 0: 100MHz; 1: 153.6MHz	VADJ	input	
LA01_N_CC	D9	FMC_40M_EN	enables on board reference	VADJ	input	
LA05_P	D11	FMC_SCL	I2C clock line	VADJ	input	
LA05_N	D12	FMC_SPI_MISO	SPI data out	VADJ	output	
LA09_P	D14	SYNCOUT1_A.D_P	JESD TX channel sync for RFIC A	LVDS	output	
LA09_N	D15	SYNCOUT1_A.D_N	JESD TX channel sync for RFIC A	LVDS	output	
LA13_P	D17	SYNCOUT0_B.D_P	JESD TX channel sync for RFIC B	LVDS	output	
LA13_N	D18	SYNCOUT0_B.D_N	JESD TX channel sync for RFIC B	LVDS	output	
LA17_P_CC	D20	RESETB_B	reset for RFIC B (active low)	VADJ	input	
LA17_N_CC	D21	GP_INTERRUPT_B	interrupt from RFIC B	VADJ	input	
LA23_P	D23	LED_BLU	enables blue LED	VADJ	input	
LA23_N	D24	NC on Rev B, FMC_EXT_DEV_CLK_SEL on Rev C	determines the functionality of (J5) EXT_10M input	VADJ	input	

LA26_P	D26	GPIOA2	GPIO bus to RFIC B	VADJ	input/ output	
LA26_N	D27	GPIOB2	GPIO bus to RFIC B	VADJ	input/ output	
TCK	D29	NC				
TDI	D30	TDI_2_TDO	Connected to D31			shorted to TDO
TDO	D31	TDI_2_TDO	Connected to D30			shorted to TDI
3P3VAUX	D32	3P3V_AUX	auxilliary 3.3V power supply	3.3V	DC in	powers FMC EEPROM
TMS	D33	NC				
TRST_L	D34	NC				
GA1	D35	GA1	geographical address 0 for EEPROM (intentionally opposite)	3.3V	input	pulled up to 3.3V
3P3V	D36	VSENSE_3V3+	main 3.3V supply input	3.3V	DC in	main 3.3V supply
3P3V	D38	VSENSE_3V3+	main 3.3V supply input	3.3V	DC in	main 3.3V supply
3P3V	D40	VSENSE_3V3+	main 3.3V supply input	3.3V	DC in	main 3.3V supply
CLK1_M2C_P	G2	CLK1_M2C_P	FPGA global clock from SKIQ clock IC port 5	LVDS	output	
CLK1_M2C_N	G3	CLK1_M2C_N	FPGA global clock from SKIQ clock IC port 5	LVDS	output	
LA00_P_CC	G6	SYNCIN0_A.D_P	JESD RX channel sync for RFIC A	LVDS	input	
LA00_N_CC	G7	SYNCIN0_A.D_N	JESD RX channel sync for RFIC A	LVDS	input	
LA03_P	G9	FMC_PPS	PPS output to FPGA fed directly from front panel PPS input	VADJ	ouput	
LA03_N	G10	FMC_SDA	I2C data line	VADJ	input/ output	
LA08_P	G12	SYNCIN1_A.D_P	JESD RX channel sync for RFIC A	LVDS	input	
LA08_N	G13	SYNCIN1_A.D_N	JESD RX channel sync for RFIC A	LVDS	input	
LA12_P	G15	TX2_ENABLE_A	enables TX2 for RFIC A	VADJ	input	
LA12_N	G16	RX2_ENABLE_A	enables RX2 for RFIC A	VADJ	input	
LA16_P	G18	SYNCIN1_B.D_P	JESD RX channel sync for RFIC B	LVDS	input	

LA16_N	G19	SYNCIN1_B.D_N	JESD RX channel sync for RFIC B	LVDS	input	
LA20_P	G21	FMC_EXT*CLK*SEL	external clock source: 0: front panel MMCX; 1: FMC*REF*IN_N/P pins on FMC connector	VADJ		
LA20_N	G22	EXT_REF_EN	set high to use HOST or EXTERNAL reference	VADJ	input	
LA22_P	G24	LED_RED	enable red LED	VADJ	input	
LA22_N	G25	LED_GRN	enable green LED	VADJ	input	
LA25_P	G27	GPIOA1	GPIO bus to RFIC A	VADJ	input/ output	
LA25_N	G28	GPIOB1	GPIO bus to RFIC B	VADJ	input/ output	
LA29_P	G30	GPIOA5	GPIO bus to RFIC A	VADJ	input/ output	
LA29_N	G31	GPIOB5	GPIO bus to RFIC B	VADJ	input/ output	
LA31_P	G33	GPIOA7	GPIO bus to RFIC A	VADJ	input/ output	
LA31_N	G34	GPIOB7	GPIO bus to RFIC B	VADJ	input/ output	
LA33_P	G36	GPIOA9	GPIO bus to RFIC A	VADJ	input/ output	
LA33_N	G37	GPIOB9	GPIO bus to RFIC B	VADJ	input/ output	
VADJ	G39	VADJ	adjustable power supply from host to mezzanine	1.8V to 2.5V	DC in	
VREF_A_M2C	H1	NC				
PRSNT_M2C_L	H2	GND	module present signal (active low)	GND		indicates presence or card to host
CLK0_M2C_P	H4	CLK0_M2C.DP	FPGA global clock from SKIQ clock IC (SYSREF) port 3	LVDS	output	
CLK0_M2C_N	H5	CLK0_M2C.DN	FPGA global clock from SKIQ clock IC (SYSREF) port 3	LVDS	output	
LA02_P	H7	SYNCOUT0_A.D_P	JESD TX channel data sync for RFIC A	LVDS	output	
LA02_N	H8	SYNCOUT0_A.D_N	JESD TX channel data sync for RFIC A	LVDS	output	
LA04_P	H10	FMC_SPI_CS_A	SPI chip select for RFIC A	VADJ	input	
LA04_N	H11	FMC_SPI_CS_9528	SPI chip select for clock IC	VADJ	input	

LA07_P	H13	FMC_SPI_CS_B	SPI chip select for RFIC B	VADJ	input	
LA07_N	H14	FMC_CLK_RESETB	clock IC reset	VADJ	input	
LA11_P	H16	TX1_ENABLE_A	enables TX channel 1 for RFIC A	VADJ	input	
LA11_N	H17	RX1_ENABLE_A	enables RX channel 1 for RFIC A	VADJ	input	
LA15_P	H19	SYNCOUT1_B.D_P	JESD TX channel data sync for RFIC B	LVDS	output	
LA15_N	H20	SYNCOUT1_B.D_N	JESD TX channel data sync for RFIC B	LVDS	output	
LA19_P	H22	TX2_ENABLE_B	enables TX channel 2 for RFIC B	VADJ	input	
LA19_N	H23	RX2_ENABLE_B	enables RX channel 2 for RFIC B	VADJ	input	
LA21_P	H25	FMC_SYSREF_REQ	SYSREF request to clock IC	VADJ	input	
LA21_N	H26	SPI_CS_DAC	SPI chip select for DAC used to warp on-board reference	VADJ	input	
LA24_P	H28	GPIOA0	GPIO bus to RFIC A	VADJ	input/ output	
LA24_N	H29	GPIOB0	GPIO bus to RFIC B	VADJ	input/ output	
LA28_P	H31	GPIOA4	GPIO bus to RFIC A	VADJ	input/ output	
LA28_N	H32	GPIOB4	GPIO bus to RFIC B	VADJ	input/ output	
LA30_P	H34	GPIOA6	GPIO bus to RFIC A	VADJ	input/ output	
LA30_N	H35	GPIOB6	GPIO bus to RFIC B	VADJ	input/ output	
LA32_P	H37	GPIOA8	GPIO bus to RFIC A	VADJ	input/ output	
LA32_N	H38	GPIOB8	GPIO bus to RFIC B	VADJ	input/ output	
VADJ	H40	VADJ	adjustable power supply from host to mezzanine	1.8V to 2.5V	DC in	

Table 7: *FMC Low Pin Count Pinout*

FMC HIGH PIN COUNT (HPC) SECTION

FMC Name	FMC Pin	Sidekiq X4 Net name	Description	Logic/Standard	Type	Comments
DP1_M2C_P	A2	DP1_M2C.DP	JESD output lane for RX SERDOUT0 on RFIC B	CML (current mode logic)	output	

DP1_M2C_N	A3	DP1_M2C.DN	JESD output lane for RX SERDOUT0 on RFIC B	CML (current mode logic)	output	
DP2_M2C_P	A6	DP2_M2C.DP	JESD output lane for RX SERDOUT1 on RFIC A	CML (current mode logic)	output	
DP2_M2C_N	A7	DP2_M2C.DN	JESD output lane for RX SERDOUT1 on RFIC A	CML (current mode logic)	output	
DP3_M2C_P	A10	DP3_M2C.DP	JESD output lane for RX SERDOUT1 on RFIC B	CML (current mode logic)	output	
DP3_M2C_N	A11	DP3_M2C.DN	JESD output lane for RX SERDOUT1 on RFIC B	CML (current mode logic)	output	
DP4_M2C_P	A14	DP4_M2C.DP	JESD output lane for RX SERDOUT2 on RFIC A	CML (current mode logic)	output	
DP4_M2C_N	A15	DP4_M2C.DN	JESD output lane for RX SERDOUT2 on RFIC A	CML (current mode logic)	output	
DP5_M2C_P	A18	DP5_M2C.DP	JESD output lane for RX SERDOUT2 on RFIC B	CML (current mode logic)	output	
DP5_M2C_N	A19	DP5_M2C.DN	JESD output lane for RX SERDOUT2 on RFIC B	CML (current mode logic)	output	
DP1_C2M_P	A22	DP1_C2M.DP	JESD input lane for TX SERDIN0 on RFIC B	CML (current mode logic)	input	
DP1_C2M_N	A23	DP1_C2M.DN	JESD input lane for TX SERDIN0 on RFIC B	CML (current mode logic)	input	
DP2_C2M_P	A26	DP2_C2M.DP	JESD input lane for TX SERDIN1 on RFIC A	CML (current mode logic)	input	
DP2_C2M_N	A27	DP2_C2M.DN	JESD input lane for TX SERDIN1 on RFIC A	CML (current mode logic)	input	
DP3_C2M_P	A30	DP3_C2M.DP	JESD input lane for TX SERDIN1 on RFIC B	CML (current mode logic)	input	
DP3_C2M_N	A31	DP3_C2M.DN	JESD input lane for TX SERDIN1 on RFIC B	CML (current mode logic)	input	
DP4_C2M_P	A34	DP4_C2M.DP	JESD input lane for TX SERDIN2 on RFIC A	CML (current mode logic)	input	
DP4_C2M_N	A35	DP4_C2M.DN	JESD input lane for TX SERDIN2 on RFIC A	CML (current mode logic)	input	
DP5_C2M_P	A38	DP5_C2M.DP	JESD input lane for TX SERDIN2 on RFIC B	CML (current mode logic)	input	
DP5_C2M_N	A39	DP5_C2M.DN	JESD input lane for TX SERDIN2 on RFIC B	CML (current mode logic)	input	
RES1	B1	NC	RESERVED			
DP9_M2C_P	B4	NC		CML (current mode logic)	output	

DP9_M2C_N	B5	NC		CML (current mode logic)	output	
DP8_M2C_P	B8	NC		CML (current mode logic)	output	
DP8_M2C_N	B9	NC		CML (current mode logic)	output	
DP7_M2C_P	B12	DP7_M2C.DP	JESD output lane for RX SERDOUT3 on RFIC B	CML (current mode logic)	output	
DP7_M2C_N	B13	DP7_M2C.DN	JESD output lane for RX SERDOUT3 on RFIC B	CML (current mode logic)	output	
DP6_M2C_P	B16	DP6_M2C.DP	JESD output lane for RX SERDOUT3 on RFIC A	CML (current mode logic)	output	
DP6_M2C_N	B17	DP6_M2C.DN	JESD output lane for RX SERDOUT3 on RFIC A	CML (current mode logic)	output	
GBT_CLK1_M2C_P	B20	GBTCLK1.DP	FPGA global clock from SKIQ clock IC port 2	LVDS	output	
GBT_CLK1_M2C_N	B21	GBTCLK1.DN	FPGA global clock from SKIQ clock IC port 2	LVDS	output	
DP9_C2M_P	B24	NC		CML (current mode logic)	input	
DP9_C2M_N	B25	NC		CML (current mode logic)	input	
DP8_C2M_P	B28	NC		CML (current mode logic)	input	
DP8_C2M_N	B29	NC		CML (current mode logic)	input	
DP7_C2M_P	B32	DP7_C2M.DP	JESD input lane for TX SERDIN3 on RFIC B	CML (current mode logic)	input	
DP7_C2M_N	B33	DP7_C2M.DN	JESD input lane for TX SERDIN3 on RFIC B	CML (current mode logic)	input	
DP6_C2M_P	B36	DP6_C2M.DP	JESD input lane for TX SERDIN3 on RFIC A	CML (current mode logic)	input	
DP6_C2M_N	B37	DP6_C2M.DN	JESD input lane for TX SERDIN3 on RFIC A	CML (current mode logic)	input	
RES0	B40	NC	RESERVED			
HA01_P_CC	E2	GPIOA11	GPIO bus to RFIC A	VADJ	input/ output	
HA01_N_CC	E3	GPIOB11	GPIO bus to RFIC B	VADJ	input/ output	
HA05_P	E6	GPIOA15	GPIO bus to RFIC A	VADJ	input/ output	

HA05_N	E7	GPIOB15	GPIO bus to RFIC B	VADJ	input/ output	
HA09_P	E9	NC on Rev B, FMC_J6_SEL0 Rev C	PPS_IN/SYSREF_IN/SYSREF_OUT selection	VADJ	input	
HA09_N	E10	NC on Rev B, FMC_J6_SEL1 Rev C	PPS_IN/SYSREF_IN/SYSREF_OUT selection	VADJ	input	
HA13_P	E12	NC				
HA13_N	E13	NC				
HA16_P	E15	NC				
HA16_N	E16	NC				
HA20_P	E18	NC				
HA20_N	E19	NC				
HB03_P	E21	NC				
HB03_N	E22	NC				
HB05_P	E24	NC				
HB05_N	E25	NC				
HB09_P	E27	NC				
HB09_N	E28	NC				
HB13_P	E30	NC				
HB13_N	E31	NC				
HB19_P	E33	NC				
HB19_N	E34	NC				
HB21_P	E36	NC				
HB21_N	E37	NC				
VADJ	E39	VADJ	adjustable power supply from host to mezzanine	1.8V to 2.5V	DC in	
PG_M2C	F1	PWR_GOOD	power good mezzanine to host	3.3V	output	
HA00_P_CC	F4	GPIOA10	GPIO bus to RFIC A	VADJ	input/ output	
HA00_N_CC	F5	GPIOB10	GPIO bus to RFIC B	VADJ	input/ output	
HA04_P	F7	GPIOA14	GPIO bus to RFIC A	VADJ	input/ output	
HA04_N	F8	GPIOB14	GPIO bus to RFIC B	VADJ	input/ output	

HA08_P	F10	GPIOA18	GPIO bus to RFIC A	VADJ	input/ output	
HA08_N	F11	GPIOB18	GPIO bus to RFIC B	VADJ	input/ output	
HA12_P	F13	NC				
HA12_N	F14	NC				
HA15_P	F16	NC				
HA15_N	F17	NC				
HA19_P	F19	NC				
HA19_N	F20	NC				
HB02_P	F22	NC				
HB02_N	F23	NC				
HB04_P	F25	NC				
HB04_N	F26	NC				
HB08_P	F28	NC				
HB08_N	F29	NC				
HB12_P	F31	NC				
HB12_N	F32	NC				
HB16_P	F34	NC				
HB16_N	F35	NC				
HB20_P	F37	NC				
HB20_N	F38	NC				
VADJ	F40	VADJ	adjustable power supply from host to mezzanine	1.8V to 2.5V	DC in	
CLK3_BIDIR_P	J2	CLK3_BIDIR.DP	FPGA global clock from SKIQ clock IC port 4	LVDS	output	
CLK3_BIDIR_N	J3	CLK3_BIDIR.DN	FPGA global clock from SKIQ clock IC port 4	LVDS	output	
HA03_P	J6	GPIOA13	GPIO bus to RFIC A	VADJ	input/ output	
HA03_N	J7	GPIOB13	GPIO bus to RFIC B	VADJ	input/ output	
HA07_P	J9	GPIOA17	GPIO bus to RFIC A	VADJ	input/ output	
HA07_N	J10	GPIOB17	GPIO bus to RFIC B	VADJ	input/ output	

HA11_P	J12	NC				
HA11_N	J13	NC				
HA14_P	J15	NC				
HA14_N	J16	NC				
HA18_P	J18	NC				
HA18_N	J19	NC				
HA22_P	J21	NC				
HA22_N	J22	NC				
HB01_P	J24	NC				
HB01_N	J25	NC				
HB07_P	J27	NC				
HB07_N	J28	NC				
HB11_P	J30	NC				
HB11_N	J31	NC				
HB15_P	J33	NC				
HB15_N	J34	NC				
HB18_P	J36	NC				
HB18_N	J37	NC				
VIO_B_M2C	J39	VDD_INTERFACE	connected to VADJ through jumper	1.8V to 2.5V	DC in	logic level on bank B for FPGA
VREF_B_M2C	K1	NC				
CLK2_BIDIR_P	K4	FMC_REF_IN.D_P	alternate reference frequency input (see FMC_EXT_CLK_SEL)	LVDS	input	
CLK2_BIDIR_N	K5	FMC_REF_IN.D_N	alternate reference frequency input (see FMC_EXT_CLK_SEL)	LVDS	input	
HA02_P	K7	GPIOA12	GPIO bus to RFIC A	VADJ	input/ output	
HA02_N	K8	GPIOB12	GPIO bus to RFIC B	VADJ	input/ output	
HA06_P	K10	GPIOA16	GPIO bus to RFIC A	VADJ	input/ output	
HA06_N	K11	GPIOB16	GPIO bus to RFIC B	VADJ	input/ output	
HA10_P	K13	NC				
HA10_N	K14	NC				

HA17_P_CC	K16	NC				
HA17_N_CC	K17	NC				
HA21_P	K19	NC				
HA21_N	K20	NC				
HA23_P	K22	NC				
HA23_N	K23	NC				
HB00_P_CC	K25	NC				
HB00_N_CC	K26	NC				
HB06_P_CC	K28	NC				
HB06_N_CC	K29	NC				
HB10_P	K31	NC				
HB10_N	K32	NC				
HB14_P	K34	NC				
HB14_N	K35	NC				
HB17_P_CC	K37	NC				
HB17_N_CC	K38	NC				
VIO_B_M2C	K40	VDD_INTERFACE	connected to VADJ through jumper	1.8V to 2.5V	DC in	logic level on band B for FPGA

Table 8: *FMC High Pin Count Pinout*

BASIC USAGE IN A HOST SYSTEM

HOST SYSTEM COMPATIBILITY

Sidekiq X4 is expected to be deployed into a host system that adheres to a general architecture in order to utilize the core FPGA reference design and associated libsidekiq software API. This general architecture is shown in Figure 5 below.

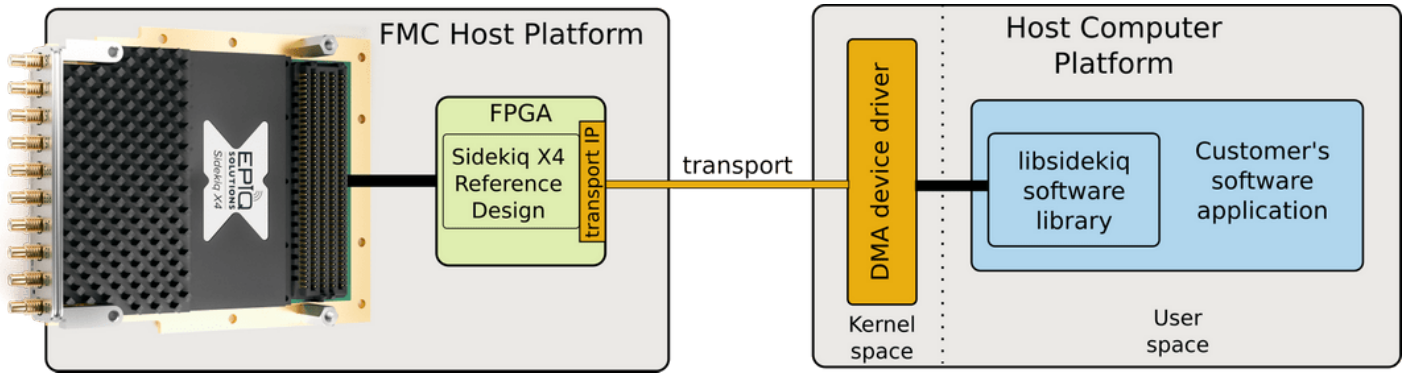

Figure 5: *General Sidekiq X4 development arhitecture*

A typical deployment scenario into a host platform is shown in Figure 6, which depicts the Sidekiq X4 plugged into a COTS PCIe FPGA board (HiTech Global's HTG-K800 [5]), mounted into a Thunderbolt 3 chassis, connected to a host computer running Linux through a Thunderbolt 3 cable. In this deployment, the FPGA on the HTG-K800 is the Xilinx Kintex Ultrascale XCKU060, and a Gen3 x4 PCIe interface native to the FPGA is utilized to provide the transport between the FPGA and host computer via the Thunderbolt 3 chassis. On the host computer, a Linux device driver supports both PCIe register reads/writes as well as DMA between the FPGA and the CPU in the host computer. The libsidekiq API then uses PCIe as the transport layer to support all of the standard Sidekiq API calls.

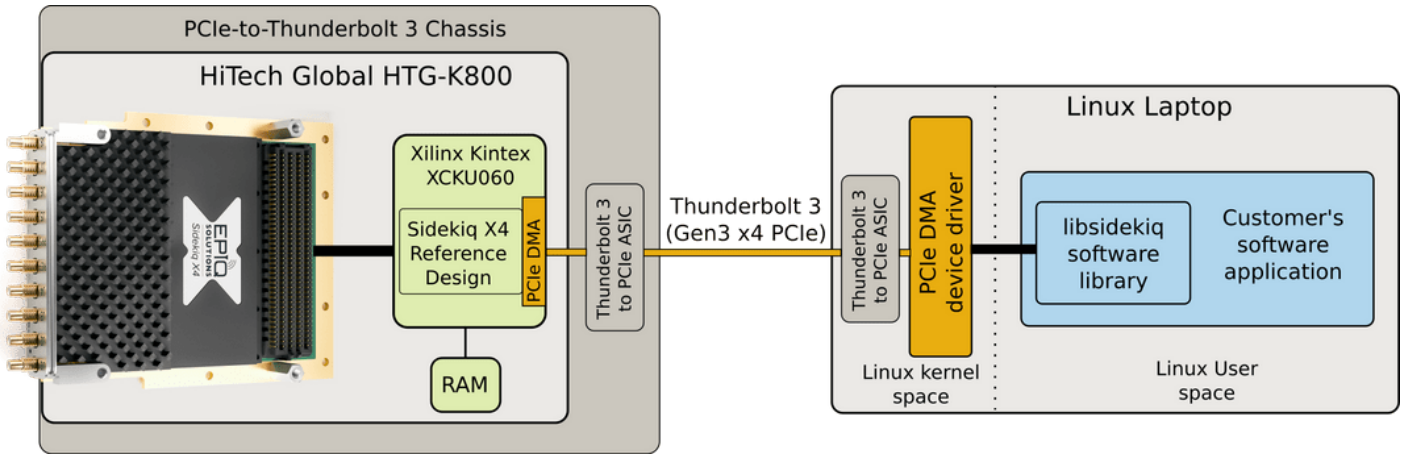

Figure 6: *Sidekiq X4 deployment architecture with PCIe carrier, Thunderbolt 3 chassis, and a host Linux PC*

In an alternate deployment scenario, Sidekiq X4 can be interfaced to a 3U VPX carrier card that hosts an integrated FPGA + CPU in a single chip, such as the Xilinx Zynq Ultrascale+ SoC. In this scenario, both the FPGA fabric required to execute the Sidekiq X4 FPGA reference design and the multi-core ARM CPU running the libsidekiq software library are located on a single device (i.e., the Zynq Ultrascale+ SoC). The transport layer used to interface between the Zynq's FPGA fabric (PL) and the Zynq's ARM CPU (PS) is an efficient AXI-based DMA interconnect. This is shown in Figure 7 below.

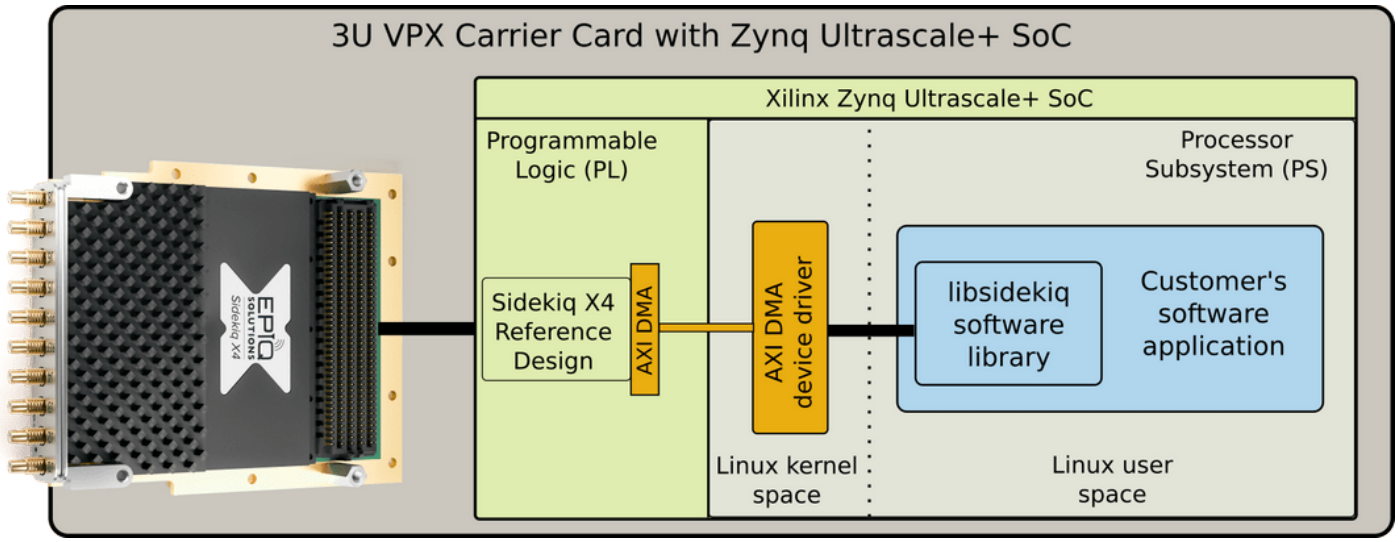

Figure 7: *Sidekiq X4 deployment architecture with a Zynq Ultrascale+ SoC*

Note that this configuration with the Zynq Ultrascale+ SoC in a 3U VPX platform could also use PCIe as the transport to interface to the VPX backplane. In this configuration, the AXI transport is no longer needed, and all transport activities would be targeting a 3U VPX computer card plugged into the 3U VPX backplane, similar to the architecture shown in Figure 6.

OPERATING SYSTEM COMPATIBILITY

Linux is the only operating system that is currently supported. Various kernel versions have been tested starting at Linux version 3.0. Sidekiq has been tested both in x86-based Linux systems as well as ARM-based Linux systems. Kernel versions prior to 3.0 (i.e., 2.6+) may also be supported.

For customers interested in doing a custom build of the Sidekiq PCIe device driver for their host platform, a license for the source code for this device driver is also available separately. Please contact Epiq Solutions for details.

Alternate operating systems, such as Windows, may also be supported in the future. Please contact Epiq Solutions for details.

POWER CONSUMPTION

The power consumption of Sidekiq X4 card is largely dependent on the number of RF channels being utilized and the sample rate at which those channels are operating. The power consumption of the card will vary between ~7W and ~11W based on this configuration. A table showing several example use cases is shown below. For each of these cases, the power consumption of the X4 card is measured by performing a DC current measurement on the 3.3V (P3V3) and 12V (12P0V) power rails provided by the FMC interface. The X4 card requires both of these rails for operation.

Test Scenario	Power Consumption (in Watts)
Test scenario #1: *rx_benchmark --handle=ALL -r 61.44e+6* -RxA1, RxA2, RxB1 and RxB2 are active: sample rate = 61.44 Msps	Current: 1048.0 mA, Voltage: 3.29 V ==> Power: 3.4427 W Current: 598.0 mA, Voltage: 12.05 V ==> Power: 7.2047 W
Test scenario #2: *rx_benchmark --handle=ALL -r 100e+6* --RxA1, RxA2, RxB1 and RxB2 are active: sample rate = 100 Msps	Current: 996.0 mA, Voltage: 3.29 V ==> Power: 3.2719 W Current: 594.0 mA, Voltage: 12.05 V ==> Power: 7.1565 W
Test scenario #3: *rx_benchmark --handle=ALL -r 250e+6* -RxA1, RxA2, RxB1 and RxB2 are active: sample rate = 250 Msps	Current: 1412.0 mA, Voltage: 3.27 V ==> Power: 4.6215 W Current: 650.0 mA, Voltage: 12.02 V ==> Power: 7.8136 W
Test scenario #4: *tx_benchmark -r 61.44e+6 --threads=4 --block-size 16380* -TxA1 is active: sample rate = 61.44 Msps	Current: 928.0 mA, Voltage: 3.29 V ==> Power: 3.0513 W Current: 562.0 mA, Voltage: 12.03 V ==> Power: 6.7597 W
Test scenario #5: *tx_benchmark -c 0 -r 100e+6 --threads=4 --block-size 16380* -TxA1 is active: sample rate = 100 Msps	Current: 876.0 mA, Voltage: 3.29 V ==> Power: 2.8838 W Current: 558.0 mA, Voltage: 12.02 V ==> Power: 6.7094 W
Test scenario #6: *tx_benchmark -r 250e+6 --threads=4 --block-size 16380* -TxA1 is active: sample rate = 250 Msps	Current: 1100.0 mA, Voltage: 3.29 V ==> Power: 3.6135 W Current: 614.0 mA, Voltage: 12.00 V ==> Power: 7.3680 W
Test scenario #7: *tx_samples -f 3e+9 --handle=A2 -s waveform.dat -r 61.44e+6 -a 20 --block-size=30718* -TxA1 and TxA2 are active: RF freq = 3000 MHz, sample rate = 61.44 Msps	Current: 918.0 mA, Voltage: 3.28 V ==> Power: 3.0147 W Current: 622.0 mA, Voltage: 12.01 V ==> Power: 7.4715 W
Test scenario #8: *tx_samples -f 3e+9 --handle=A2 -s waveform.dat -r 100e+6 -a 20 --block-size=30718* -TxA1 and TxA2 are active: RF freq = 3000 MHz, sample rate = 100 Msps	Current: 1234.0 mA, Voltage: 3.28 V ==> Power: 4.0475 W Current: 626.0 mA, Voltage: 11.98 V ==> Power: 7.5001 W
Test scenario #9: *tx_samples -f 3e+9 --handle=A2 -s waveform.dat -r 250e+6 -a 20 --block-size=30718* -TxA1 and TxA2 are active: RF freq = 3000 MHz, sample rate = 250 Msps	Current: 1208.0 mA, Voltage: 3.28 V ==> Power: 3.9671 W Current: 682.0 mA, Voltage: 11.98 V ==> Power: 8.1710

Table 9: *Example power consumption measurements for Sidekiq X4*

THERMAL DISSIPATION

Effective use of Sidekiq X4 in a system also requires consideration of an appropriate thermal dissipation solution. Sidekiq X4 can be integrated into a variety of different host systems with different thermal profiles (i.e., forced air, natural convection, etc), and the end user is required to perform their own system analysis to determine what level of thermal dissipation is appropriate for their use-case. For a standard convection cooled deployment, the required air flow over the heatsink on the card is TBD LFM. Sidekiq X4 uses components that are rated for operation to +85 deg C, and thus the end user must ensure that the temperature reported by the on-board temperature sensor does not exceed +85 deg C. The on-board temperature of the card can be queried through a temperature sensor, which can then be reported up to the host software application via the libsidekiq API. **Exceeding the maximum rated temperature of +85 deg C may damage the Sidekiq X4 card and/or accelerate failure of the card.**

The following are the key circuit elements dissipating power on Sidekiq X4. The listed power values represent **worst case** at 100% duty cycle; actual power dissipation will be application dependent.

IC	Part Number	Reference	Pdiss	Side
RFIC	ADRV9009	U1A, U1B	6.1W, each	top
Clock Driver	AD9528	U2	1.4W	bottom
Power Supply	MPM3630	U29A, U29B	0.5W each	bottom
Power Supply	MPM3840	U15A, U15B	0.3W each	bottom
Power Supply	MPM3830	U23A, U23B	0.2W each	bottom

Table 10: *Sidekiq X4 component power consumption*

The side with the FMC connector is designated "top". Component locations are shown below.

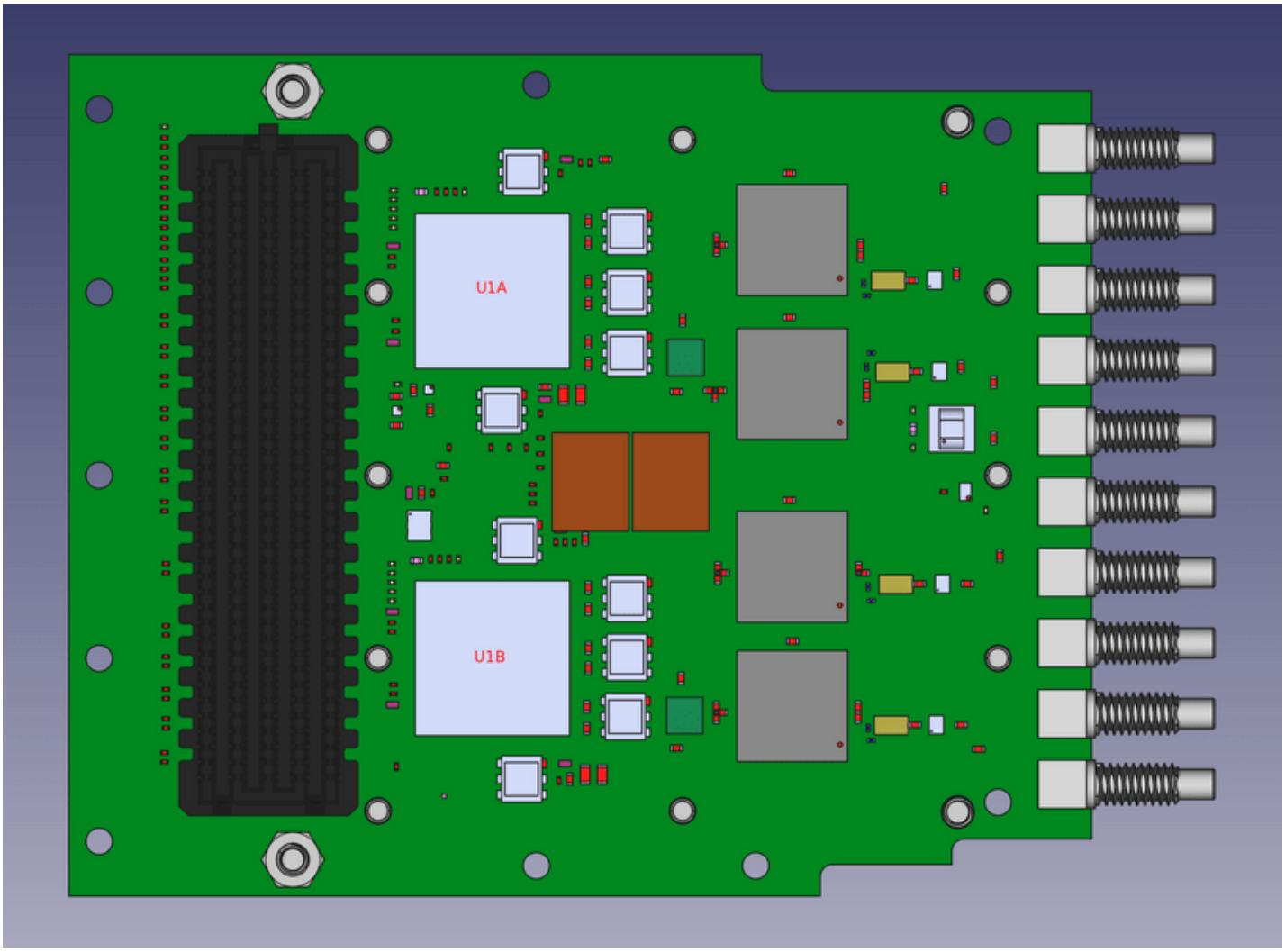

Figure 8: *Sidekiq X4 Top and Bottom Sides*

- The thermal gap pad material used on the X4 RFICs is Bergquist Gap Pad P/N: GPVOUS-0.040-00
- The thermal pads are 0.50" x 0.50" x 0.060" thick and 0.040" thick respectively and are compressed around 50%.
- **For air-cooled designs, the heat is primarily conducted directly away from the top surfaces of the RFICs as delivered with the heat sink/shield. The heat sink/shield is secured to the perimeter exposed metal with 10 screws which does also provide some conduction to the heat sink.**

JTAG ACCESS ON SIDEKIQ

The standard FMC interface includes pins for addressing JTAG devices local to the card. On Sidekiq X4, there are no devices on the JTAG chain. The TDI line is directly connected to the TDO line to allow the JTAG chain to pass through the FMC interface.

SIDEKIQ X4 MECHANICAL OUTLINE

A dimensioned mechanical drawing of Sidekiq X4 in convection cooled form is shown in Figure 9. In addition, a 3D model (in STP format) is also available. Please contact Epiq Solutions for this model.

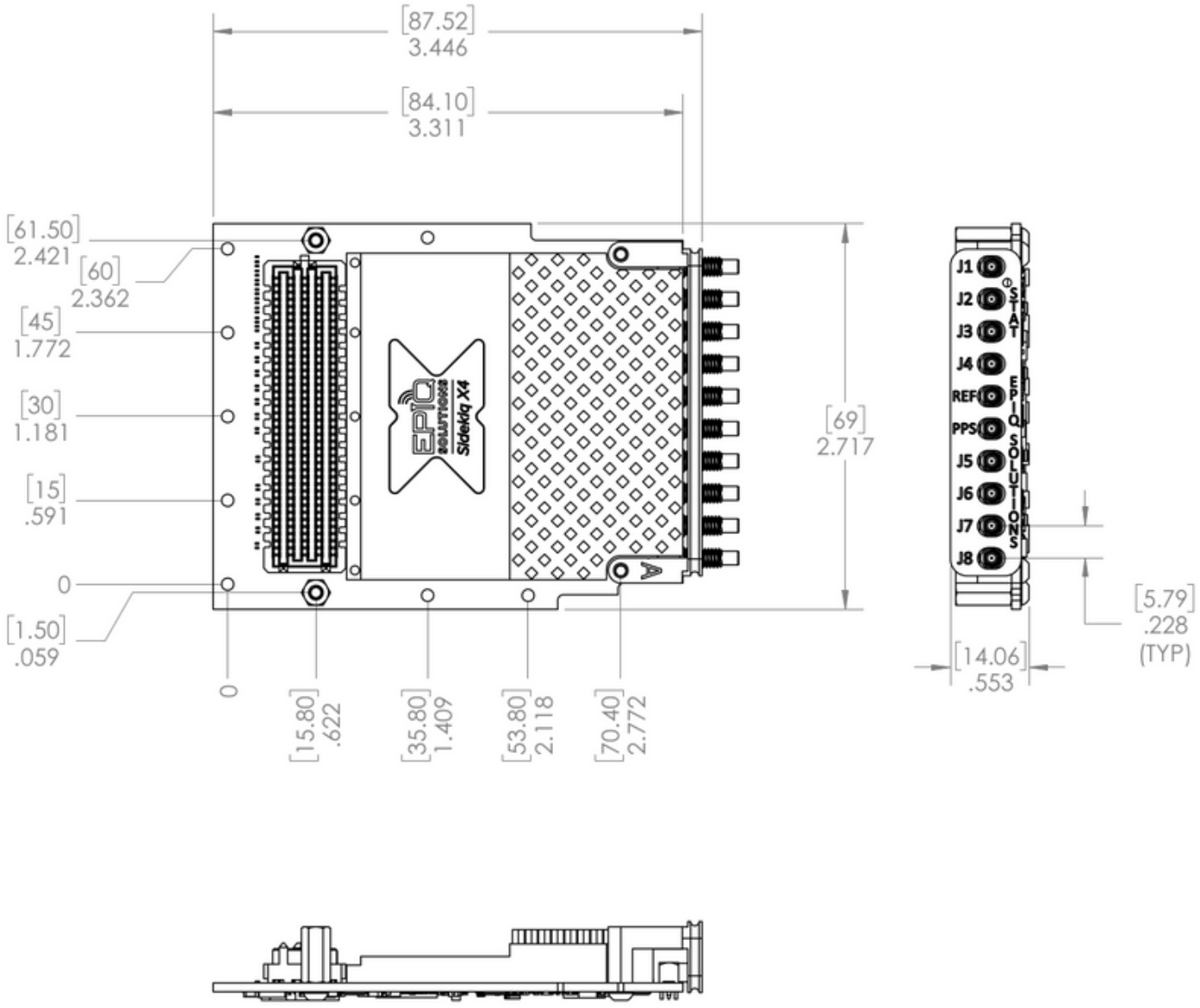

Figure 9: *Sidekiq X4 Mechanical Outline*

Conduction cooled variants of Sidekiq X4 are also supported, which require an alternate heatframe for cooling as well as a replacement of the front panel SSMC connectors with footprint compatible MMCX or SMP connectors. Please contact Epiq Solutions for details.

SIDEKIQ X4 THUNDERBOLT 3 PLATFORM

OVERVIEW

The Sidekiq X4 Platform Development Kit (PDK) includes one Sidekiq X4 card integrated on to a COTS FPGA PCIe card (Hi Tech Global HTG-K800 [5]) with a Xilinx Kintex Ultrascale XCKU060 FPGA. This PCIe card is then installed in to a COTS Thunderbolt 3 chassis that converts the Gen3 x4 PCIe interface available on the HTG-K800 into Thunderbolt 3, and presents this interface through the Thunderbolt 3 interface accessible on the chassis. A Thunderbolt 3 cable can then connect the chassis to a Linux host PC, where the system appears as a PCIe device plugged into the system. A picture of Sidekiq X4 + HTG-K800 PCIe card installed into the Thunderbolt 3 chassis and connected to a host laptop is shown in Figure 9.

Figure 10: *Sidekiq X4 & HTG-K800 FPGA host board installed into a Thunderbolt 3 chassis, interfaced to a laptop via a Thunderbolt 3 cable*

BASIC USAGE THE SIDEKIQ X4 THUNDERBOLT 3 PLATFORM

The following steps can be followed to perform a basic RF recording (using the rx_samples test application) and RF playback (using the tx_samples test application) with the Sidekiq X4 Thunderbolt 3 platform that ships with the PDK:

Step 1. With the Sidekiq X4 Thunderbolt 3 platform powered on *first* (using the provided DC power brick for the Thunderbolt 3 chassis), connect the TB3 chassis to the laptop with the provided TB3 cable and power on the laptop *last*. The TB3 chassis will fully power-on when the laptop is connected and powered-up.

Step 2. Log into Ubuntu laptop with the user credentials:

```
Username: sidekiq
Password: sidekiq
```

Step 3. Launch a terminal window or by pressing Ctrl-Alt-T.

Step 4. Navigate to `/home/sidekiq/sidekiq_image_current/test_apps/`

Step 5. A user can perform an RF recording of I/Q samples using the default configuration by executing the rx_samples application as follows:

```
./rx_samples -d <FILE>
```

This command will save I/Q samples to a file named <FILE>.a1 using default values for RF frequency, sample rate, and other parameters. The data is stored in the file as 16-bit I/Q pairs with 'I' samples stored in the upper 16-bits of each word, and 'Q' samples stored in the lower 16-bits of each word. Additional available options are described by executing:

```
./rx_samples -h
```

Configuration of frequency, sample rate, bandwidth, number of samples, and more are available with additional command line parameters.

Step 6. A file of I/Q samples can also be transmitted out by running the tx_samples application using the default configuration as follows:

```
./tx_samples -s <FILE>
```

This application expects the same I/Q file format for samples as produced by the rx_samples application. Additional available options are described by executing:

```
./tx_samples -h
```

Configuration of frequency, sample rate, bandwidth, timestamp modes, block size, and more are available with additional command line parameters. It is highly recommended that a user profile their system for an adequate transmit block and mode configuration by running tx_benchmark (more details in the Sidekiq SDK Manual, Appendix 8 - Assessing Throughput Performance)

Both rx_samples and tx_samples are test applications to serve as examples of how to use the libsidekiq API. The source code for these test applications and others are distributed with the SDK at /home/sidekiq/sidekiq_sdk_vX, where 'X' represents the version of the release.

ACCESSING JTAG ON THE SIDEKIQ X4 THUNDERBOLT 3 PLATFORM

For customers adding their own custom FPGA blocks in the “user_app” area of the Sidekiq X4 reference design, it can often be useful to access JTAG to monitor signals in the FPGA through Xilinx's Chipscope software running on a separate PC. The HTG-K800 FPGA PCIe card provides access to the JTAG port of the XCKU060 FPGA through a 2x7 header on the top side of the board. A standard Xilinx JTAG USB platform cable, such as the HW-USB-II-G, can be utilized to access JTAG on the FPGA. In order to access this JTAG header, the Thunderbolt 3 platform must first be powered down, and the outer shell of the Thunderbolt 3 chassis must be removed by unscrewing the two front thumbscrews and carefully sliding the internal board stack out. Once the shell is removed, the JTAG header is accessible, as shown in Figure 10 below.

> Note: it is critical that the user exercise proper electrical safety measures and ESD protection when interacting with open frame electronics. Failure to do so can permanently damage both the Sidekiq X4 card as well as the HTG-K800 FPGA board.

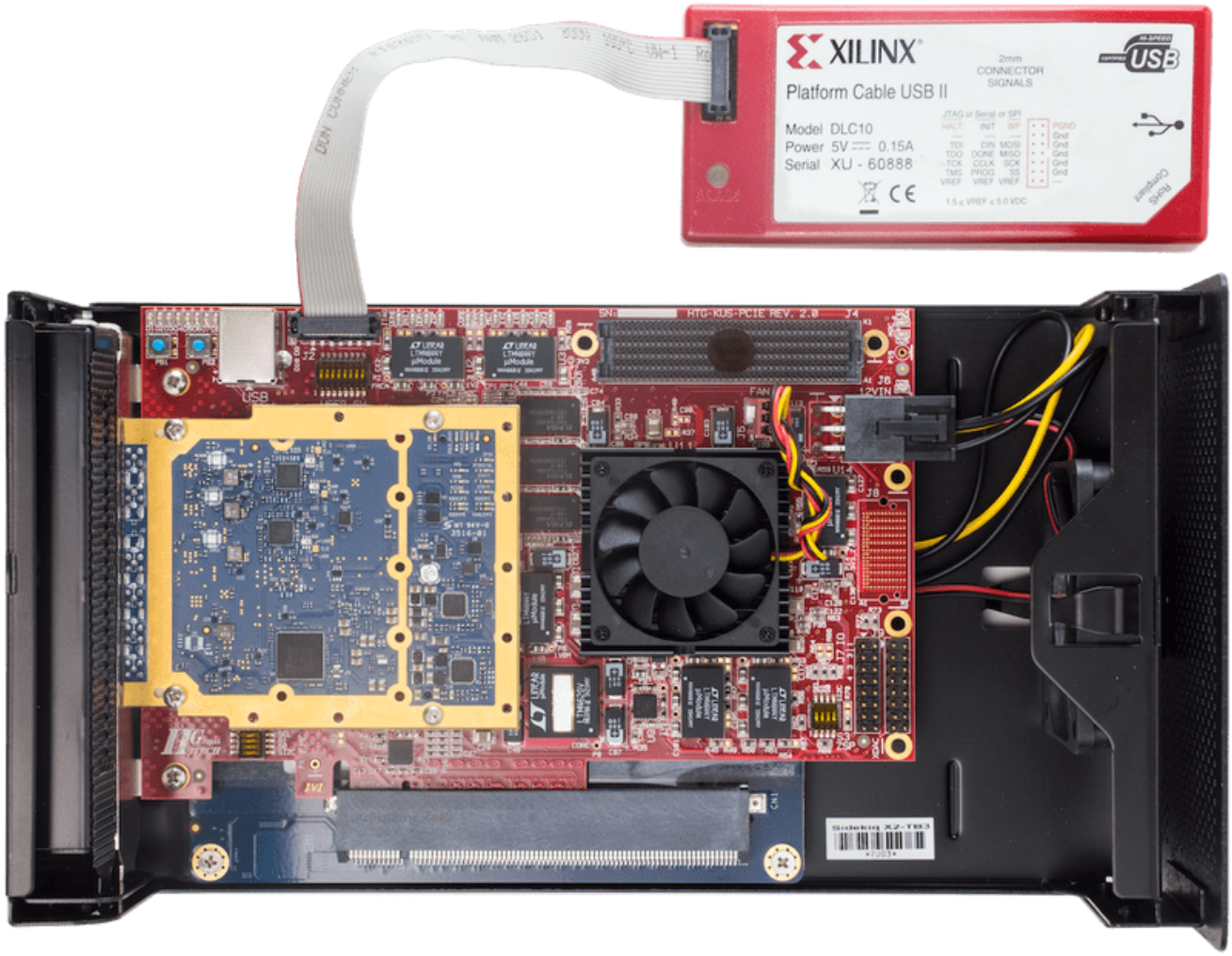

Figure 11: *JTAG port access on the Sidekiq X4 Thunderbolt 3 platform*

Once the JTAG cable is installed, the Thunderbolt 3 chassis cover can be carefully replaced, as shown in Figure 11, with the JTAG cable coming through the front panel of the unit. This ensures that the airflow from the internal fans is properly ducted over the critical components including Sidekiq X4.

Figure 12: *Thunderbolt 3 chassis closed up with Xilinx JTAG interface installed*

With the Thunderbolt 3 chassis reassembled, the user can resume normal usage of the system.

APPENDIX A – SIDEKIQ X4 STATEMENT OF VOLATILITY

Model	Sidekiq X4
Part Number	ES024-xxx
Manufacturer	Epiq Solutions
Address	3740 Industrial Avenue Rolling Meadows, IL 60008

Table 11: *Model, Part Number, and Manufacturer Info*

Memory Type	Memory Size	User Modifiable	Purpose	Process to Clear
AD9528 clock generator	1.3 KB	Yes	Clock control registers	Power-off
ADRV9009	???	Yes	RFIC ARM memory and configuration space	Power-off

Table 12: *Sidekiq X4 Volatile Memory*

Memory Type	Memory Size	User Modifiable	Removable	Purpose	Process to Clear
EEPROM	32 Kbit	No	No	Holds product information for identifying FMC device (part#, serial#, and power requirements)	Must be returned to factory to clear
EEPROM	512 Kbit	Yes	No	Holds factory calibration data and user configuration settings: ref_clock selection	Factory calibration data is read only and must be returned to factory to clear. Ref_clk setting is read/write via API

Table 13: *Sidekiq X4 Non-Volatile Memory*

APPENDIX B – FAILURE RATE & MTBF

Listed below is the Failure Rate and MTBF for the ES024-211-01-B Sidekiq X4 Assembly.

The Calculations are derived from Relyence Reliability Software and based off a fixed/ground/controlled operating environment with an ambient temperature of 25°C.

Part Number	ES024-211-01-B
Description	Sidekiq X4 Assembly
Failure Rate (fpmh)	0.755794
MTBF (hours)	1,323,112.23
Calculation Model	Telcordia Issue 4
Operating Environment	Fixed/Ground/Controlled
Ambient Temperature	25°C

Table 14: *Sidekiq X4 Failure Rate & MTBF*