Sidekiq™ X2

RF Transceiver • High Performance

HARDWARE USER MANUAL

V1.0 - NOVEMBER 11, 2020

CHANGELOG

Revision	Date	Description	Author
0.1	2017-08-10	Pre-release draft, initial version	Barry L
0.2	2017-09-07	Subtandital updates in content; Added full pin map; Added Rx pre-select filter plot	Barry L
0.3	2017-09-15	Updates after internal review; ready for public release	Barry L
0.4	2020-03-09	Updated sections 7.1, 7.3, 8, 8.7, 8.8, 10.2, 10.3, 11, table12. Added table 3, sections 13, 14	Barry L
1.0	2020-11-11	Markdown conversion, table updates	Barry L

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INTRODUCTION

This document provides an overview and usage details of Epiq Solutions' Sidekiq X2 multichannel RF transceiver card [1], a VITA 57.1 compliant FPGA mezzanine card (FMC) utilizing the high pin count (HPC) interface. Sidekiq X2 provides the entire "antenna-to-bits" high performance RF signal chain in a single card, allowing a customer to radically shorten their typical RF platform development cycle. Sidekiq X2 can interface to any FMC HPC host system, where an FPGA and additional follow on processing would be executed. Epiq Solutions provides an FPGA reference design as well as software drivers, libraries, and test applications to demonstrate the usage of Sidekiq X2 interfaced to a COTS FMC host platform with a PCIe interface to a host computing system. This reference design, as well as the software drivers, libraries, and test applications, can then be ported to other FMC host carrier systems for custom deployment scenarios.

The following topics will be discussed:

- Overview of the Sidekiq X2 hardware interfaces
- Sidekiq X2 usage/integration options
- Sidekiq X2 example usage in the FMC host platform reference design

All documentation and support for Sidekiq X2 is provided through Epiq Solutions' support website [2], please note that it is necessary to register prior to accessing the relevant information for your purchase.

LEGAL CONSIDERATIONS

The Sidekiq X2 is distributed all over the world. Each country has its own laws governing reception and transmission of radio frequencies. Each user of Sidekiq X2 and associated software is solely responsible for insuring that it is used in a manner consistent with the laws of the jurisdiction in which it is used. Many countries, including the United States, prohibit the transmission and reception of certain frequency bands, or receiving certain transmissions without proper authorization. Again, the user is solely responsible for the user's own actions.

PROPER CARE AND HANDLING

Each Sidekiq X2 card is fully tested by Epiq Solutions before shipment, and is guaranteed functional at the time it is received by the customer, and ONLY AT THAT TIME. Improper use of the Sidekiq X2 card can cause it to become non-functional. In particular, a list of actions that may cause damage to the hardware include the following:

- Handling the unit without proper static precautions (ESD protection) when the housing is removed or opened up
- Inserting or removing Sidekiq X2 from a host system when power is applied to the host system
- Connecting a transmitter to the RX port without proper attenuation
- Executing custom software and/or an FPGA bitstream that was not developed according to guidelines

The above list is not comprehensive, and experience with the appropriate measures for handling electronic devices is required.

REFERENCES

1. Sidekiq X2 Product Page

https://epiqsolutions.com/rf-transceiver/sidekiq-x2

2. Epiq Solutions Support Page

   https://support.epiqsolutions.com

3. VITA website

   https://www.vita.com

4. Analog Devices' AD9371 Wideband Transceiver Product Page

   http://www.analog.com/en/products/rf-microwave/integrated-transceivers-transmitters-receivers/wideband-transceivers-ic/ad9371.html

5. HiTech Global's Product Page for the HTG-K800 FPGA PCIe Carrier Card

   http://www.hitechglobal.com/Boards/Kintex-UltraScale.htm

TERMS AND DEFINITIONS

Term	Definition
A/D	Analog to Digital converter
D/A	Digital to Analog converter
dB	Decibel
dBm	Decibels (dB) with reference to one milliwatt (mW).
ESD	ElectroStatic Discharge
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
GPS	Global Positioning System
HPC	High Pin Count (a variant of the VITA 57.1 electrical interface)
I/Q	In-Phase / Quadrature Phase
JTAG	Joint Test Action Group
KHz	Kilohertz
LED	Light Emitting Diode
LFM	Linear Feet per Minute
LNA	Low Noise Amplifier
LPC	Low Pin Count (a variant of the VITA 57.1 electrical interface)
MHz	Megahertz
MMCX	Micro-Miniature Coaxial RF Connector
ObsRx	Observation Receiver
PC	Personal Computer
PDK	Platform Development Kit
PPS	Pulse Per Second
RF	Radio Frequency
Rx	Receive
SDK	Software Development Kit
SDR	Software Defined Radio
SMP	Sub-Miniature push-on RF connector
SSH	Secure SHell

SSMC	A smaller version of the SubMiniature type C RF connector
TCXO	Temperature Compensated Crystal Oscillator
Tx	Transmit
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VITA	The standards body governing a variety of electro-mechanical specifications for computing systems (see [3] for details).

Table 1: *Terms and Definitions*

HARDWARE OVERVIEW

Sidekiq X2 is a high performance multichannel RF transceiver card providing a complete "antenna-to-bits" solution in a VITA 57.1 FPGA mezzanine card (FMC) form factor. Sidekiq X2 leverages Analog Devices' AD9371 wideband transceiver RFIC [4] to provide the core functionality of the card. The capability of the card is further enhanced with on-board circuitry to extend the RF tuning range, provide RF pre-select filtering on the RF receivers, support external synchronization inputs, and other features only found on Sidekiq X2. The key highlights of Sidekiq X2 are enumerated below:

- VITA 57.1 FMC compliant card providing a high pin count (HPC) interface
- RF tuning range from 1 MHz to 6 GHz
- Phase coherent RF receiver pair with common LO
- Third independently tunable RF receiver
- Phase coherent RF transmitter pair with common LO
- Supports RF channel bandwidths up to 100 MHz
- 16-bit A/D converters supporting sample rates up to 122.88 Msamples/sec
- 14-bit D/A converters supporting sample rates up to 245.76 Msamples/sec
- Seven-band RF pre-select filters on all RF receivers
- On-board 10 MHz TCXO reference clock (0.2 PPM stability)
- Accepts external 10 MHz and PPS inputs for synchronization to user provided reference signals
- Weight: 2.7 oz
- Power: 4-10 W (application dependent)
- Size: 84.1mm x 69mm

Figure 1: *Sidekiq X2 card (with heatsink / RF shield installed)*

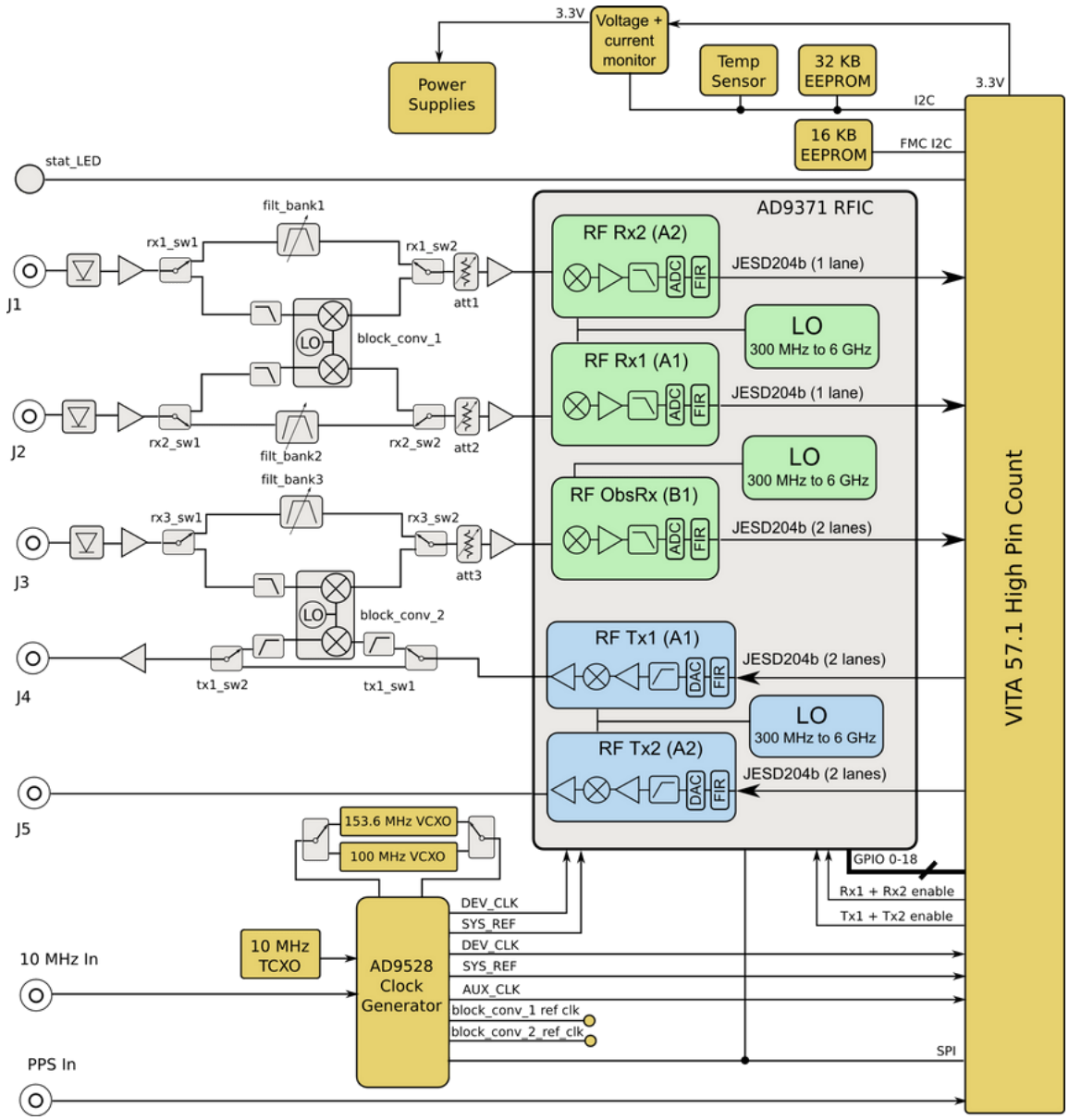


Figure 2: *Sidekiq X2 block diagram*

HARDWARE SPECIFICATION

RF RECEIVER SPECIFICATION (RX1, RX2, OBSRX)

RF Input	50 ohms (MMCX, SMP and SSMC options)
Architecture	Zero-IF (direct conversion)
Tuning Range	75 MHz to 6 GHz, able to capture 1 MHz to 6 GHz
Tuning Step Size	2.3 Hz
Tuning Time	~ 1 ms to 2.5 ms, contact Epiq Solutions' support [2] for more detailed information
Typical Noise Figure	6-8 dB below 3 GHz, 8-10 dB above 3 GHz
Spurious-Free Dynamic Range	~ 70 – 80 dB typical
Typical IIP3 (at 8 dB noise figure)	+5 to +10 dBm
Gain Control Range	0 to 30 dB (Rx1 and Rx2); 0-18 dB (ObsRx); 1 dB steps
Gain Control Modes	Manual or AGC
A/D Converter Sample Rate	Up to 122.88 Msamples/sec
A/D Converter Sample Width	16 bits
Typical I/Q Balance	70 dB
A/D JESD204b Lane Rate	Up to 6.144 Gbps
# of JESD204b Lanes Utilized	Rx1, Rx2: 1 lane ObsRx: 1 or 2 lanes (Fs dependent)
Max RF input signal (without damage)	+25 dBm
RF full scale input (at max gain)	~ -30 dBm to -20 dBm, (frequency dependent)
RF Pre-Select Filter Passbands	Automatically selected when tuning the RF receiver; see Figure 3 for passband details

Table 2: *rx specification*

RF TRANSMITTER SPECIFICATION (TX1, TX2)

RF Output	50 ohms (MMCX, SMP and SSMC options)
Architecture	Zero-IF (direct conversion)

Tuning Range	Tx1: 1 MHz* to 6 GHz Tx2: 300 MHz to 6 GHz **Tx1 transmit frequency between 1 MHz and 300 MHz shares an LO source for block conversion with the ObsRx port*
Tuning Step Size	2.3 Hz
Tuning Time	~ 1 to 2.5 ms, contact Epiq Solutions' support [2] for more detailed information
Gain Control Range	0 to 42 dB, 1 dB steps
Max RF Transmit Output Power	**Tx1**: +10 dBm to +15 dBm (<3 GHz) +3 dBm to +10 dBm (>3 GHz) **Tx2**: 0 dBm to +3 dBm (<3 GHz) -10 dBm to 0 dBm (>3 GHz)
Typical OIP3	+26 dBm
D/A Converter Sample Rate	Up to 245.76 Msamples/sec
D/A Converter Sample Width	14 bits
Typical I/Q Balance	>60 dB
D/A JESD204b Lane Rate	Up to 6.144 Gbps
# of JESD204b Lanes Utilized	Tx1: 1 or 2 lanes (sample rate dependent) Tx2: 1 or 2 lanes (sample rate dependent)

***Table 3:** tx specification*

CLOCK/SYNCHRONIZATION SPECIFICATION

Port	50 ohms (MMCX, SMP and SSMC options)
On Board Reference Clock	40 MHz TCXO (0.2 PPM stability) Part #: Abracon ASVTX12
External Reference Clock Input Frequency	10 MHz
External Reference Clock Input Power Range	-5 dBm to +10 dBm
On Board VCXO for DEV_CLK	Software switchable between two options (both populated on board): Option 1: 153.6 MHz (PN: Bliley BCVCB153M6) Option 2: 100 MHz (PN: Bliley BCVCB100)
PPS Input Level	Vadj logic level (1.8V or 2.5V), 5V tolerant

***Table 4:** clock/sync specification*

HARDWARE SPECIFICATION

Component Temperature Rating	-40 deg C to +85 deg C
FMC Interface Type	High Pin Count
FMC Card Dimensions	84.1 mm x 69 mm
FMC Stacking Height	8.5 mm
Weight	2.7 oz
Temperature Sensor	-55 deg C to +125 deg C (+/- 2 deg C resolution) P/N: Texas Instruments TMP100
FMC (12P0V)	+12 V
FMC (P3V3)	+3.3 V
FMC Vadj Support	1.8V or 2.5V

Table 5: *hardware specification*

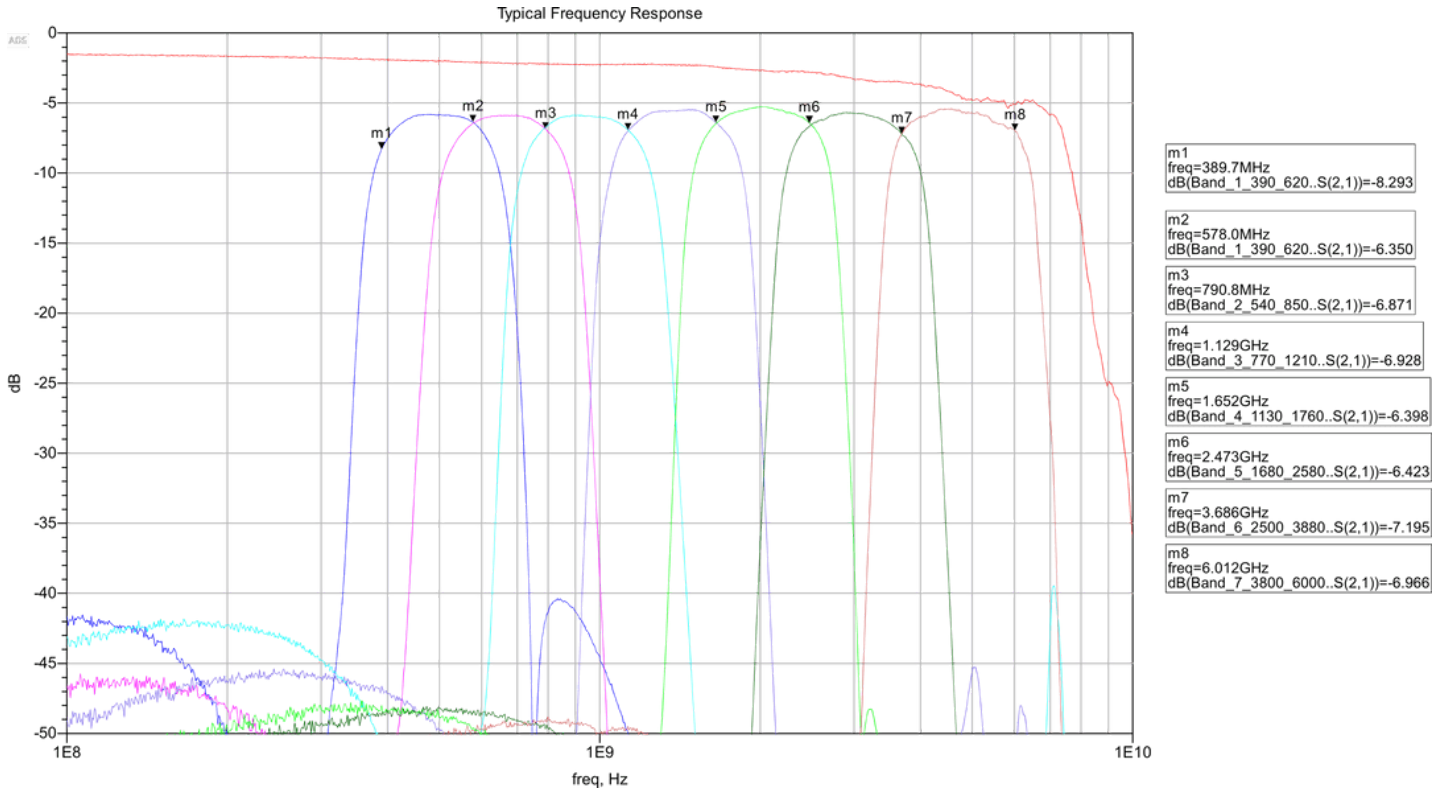


Figure 3: *Rx pre-select filter passband plot (filtering used on Rx1, Rx2, and ObsRx)*

HARDWARE INTERFACES

Sidekiq X2 provides is a standard VITA 57.1 compliant FMC card, and thus has a specific set of externally accessible hardware interfaces that are available to a user when the card is integrated into a system. Each of these hardware interfaces are enumerated in Figure 4, and are defined below.

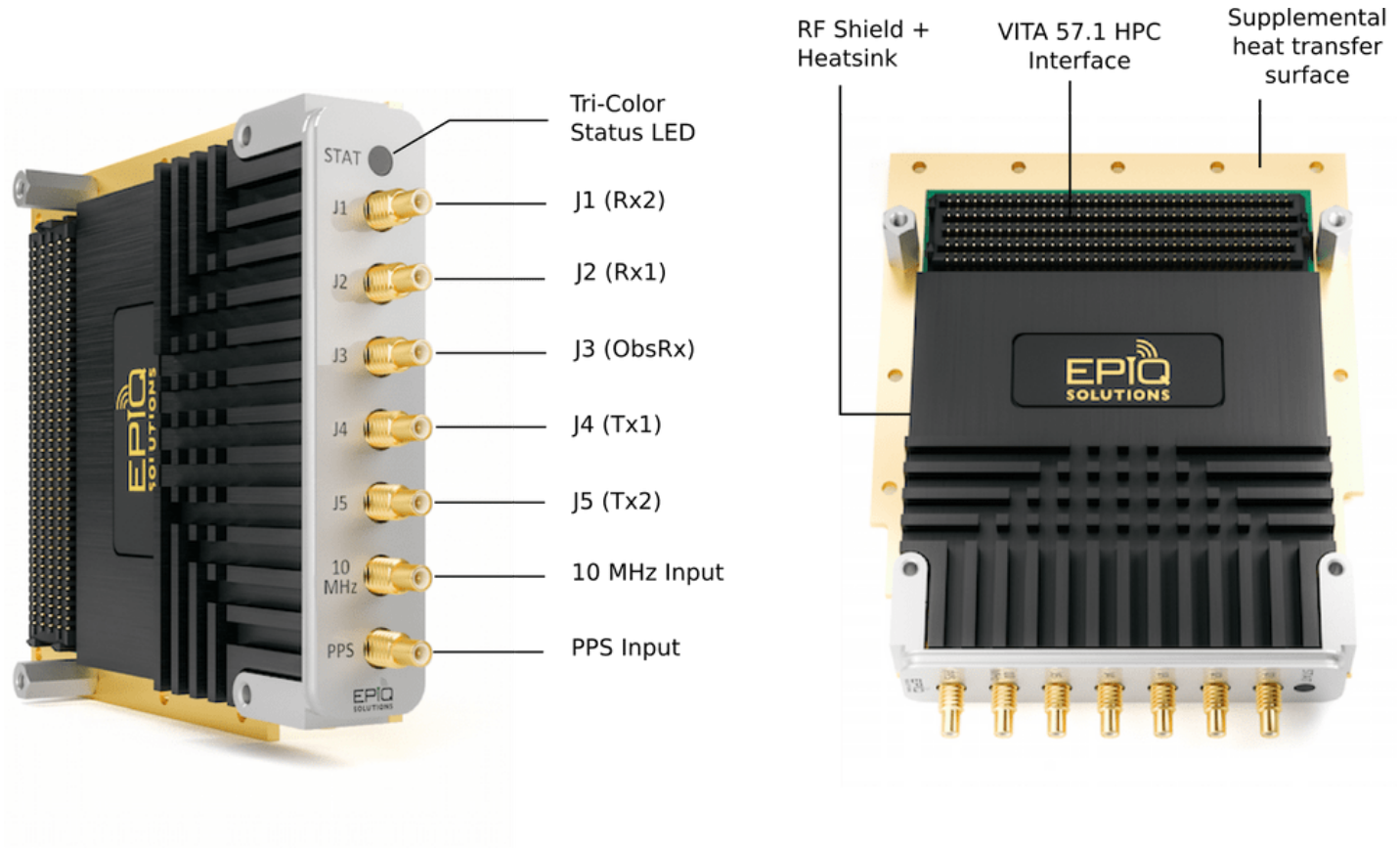


Figure 4: *Sidekiq X2 user accessible I/O*

TRI-COLOR STATUS LED

The Tri-Color Status LED is a triple LED capable of emitting red, green, and blue light through the front panel light pipe. This LED is controlled through three GPIO signals (one for each color) accessible through the VITA 57.1 electrical interface. By default, this LED illuminates blue to indicate the card is powered up.

J1 (RX2)

The J1 (Rx2) interface is an SSMC jack connector that provides an RF input path for the Rx2 antenna port. This antenna port is capable of receiving signals between 1 MHz and 6 GHz. The RF

receiver associated with this antenna port shares a common LO with J2 (Rx1). The impedance of this port is 50 ohms. This port is also referenced by its handle name (RxA2) in the libsidekiq API.

J2 (RX1)

The J2 (Rx1) interface is an SSMC jack connector that provides an RF input path for the Rx1 antenna port. This antenna port is capable of receiving signals between 1 MHz and 6 GHz. The RF receiver associated with this antenna port shares a common LO with J1 (Rx2). The impedance of this port is 50 ohms. This port is also referenced by its handle name (RxA1) in the libsidekiq API.

J3 (OBSRX)

The J3 (ObsRx) interface is an SSMC jack connector that provides an RF input path for the ObsRx antenna port. This antenna port is capable of receiving signals between 1 MHz and 6 GHz, and can be tuned independently of Rx1 and Rx2. The impedance of this port is 50 ohms. This port is also referenced by its handle name (RxB1) in the libsidekiq API.

J4 (TX1)

The J4 (Tx1) interface is an SSMC jack connector that provides an RF output path for the Tx1 antenna port. This antenna port is capable of transmitting signals between 1 MHz and 6 GHz, and shares a common LO with J5 (Tx2). The impedance of this port is 50 ohms. This port is also referenced by its handle name (TxA1) in the libsidekiq API.

J5 (TX2)

The J5 (Tx2) interface is an SSMC jack connector that provides an RF output path for the Tx2 antenna port. This antenna port is capable of transmitting signals between 300 MHz and 6 GHz, and shares a common LO with J4 (Tx1). The impedance of this port is 50 ohms. This port is also referenced by its handle name (TxA2) in the libsidekiq API.

INPUT - 10 MHZ

The 10 MHz Input port is an SSMC jack connector that accepts an external 10 MHz input signal for the purpose of phase locking the on board reference clock. The acceptable signal level for this external 10 MHz input is between -5 dBm and +10 dBm. By default, Sidekiq X2 has an internal

reference clock on board that is used for phase locking the system. In order to use an external 10 MHz reference input, the libsidekiq software API provides a function call to disable on the on-board 10 MHz reference and lock on to this external 10 MHz reference input.

PPS INPUT

The PPS Input port is an SSMC jack connector that accepts a pulse per second (PPS) input signal for the purpose of providing a temporal frame of reference relative to this PPS edge. This PPS signal is routed through a SN74LVC2G17YZPR buffer directly to the FMC electrical interface, and thus routes directly into the FPGA on the host system. The PPS edge is expected to be a rising edge with a fast slew rate, with a logic level high defined as any voltage between 0.85V and 5V, dependent on Vadj (+1.8V / +2.5V). This PPS signal is used by the Sidekiq X2 FPGA reference design to latch the digital timestamp of when the PPS edge occurs in the FPGA, and can then be queried by the libsidekiq software API. It is also possible to coordinate other actions to take place based on the occurrence of a PPS edge, such as starting Rx or Tx streaming.

> **Note:** for conduction cooled applications, MMCX or SMP connectors are available. Contact Epiq Solutions for details.

RF SHIELD + HEATSINK

The RF shield/heatsink provides both RF isolation from spurious RF signals, while also providing a thermal dissipation path for the card when used in convection cooled application. A minimum air flow of TBD LFM is required to ensure that the heat generated by the card is adequately dissipated.

VITA 57.1 HPC CONNECTOR

The VITA 57.1 HPC connector is the primary electrical interface for connecting Sidekiq X2 to a host system. The complete pin mapping for signals accessible through this HPC interface on Sidekiq X2 is defined in the FMC High Pin Count (HPC) Section..

> Note: It is assumed that the standard Sidekiq X2 FPGA reference design + libsidekiq software API is being utilized by the host system. This reference design + software API provides all of the infrastructure and control necessary to control the operation of the card, as well as stream data between the card and the host system. The Sidekiq X2 FPGA reference design + libsidekiq software API can be ported to alternate host platforms other than the PDK reference platform. Please contact Epiq Solutions for details.

SUPPLEMENTAL HEAT TRANSFER SURFACE

The Supplemental Heat Transfer Surface provides an additional thermal relief surface for the FMC card. This area surrounding the edge of the card is defined in the VITA 57.1 specification for the purpose of thermal relief, and can be used in conduction cooled deployments. For convection cooled deployments with the appropriate airflow moving over the RF shield + heatsink, this supplemental heat transfer surface is unused.

FMC PIN MAP

The following table provides the definition of all of the pins utilized on the FMC interface of Sidekiq X2. This includes pins allocated to both the low pin count (LPC) portion of the connector, as well as the high pin count (HPC) portion of the connector. Additional details of the FMC electrical interface can be found in the VITA 57.1 specification [3]. Note: the definition and allocation of these pins typically have a specific meaning in the context of both the FMC specification, and more importantly, the Sidekiq X2 FPGA reference design delivered with the Sidekiq X2 PDK. Epiq Solutions provides support for Sidekiq X2 when used in conjunction with the Sidekiq X2 FPGA reference design and associated libsidekiq software library.

FMC LOW PIN COUNT (LPC) SECTION

FMC Signal Name	FMC Pin	FMC Description	Sidekiq X2 Net Name	Description	Logic Standard, I/O Type
TRST_L	D34	JTAG reset		N/C	
TCK	D29	JTAG clock		N/C	
TDO	D31	JTAG data out		Connected to D30	
TDI	D30	JTAG data in		Connected to D31	
TMS	D33	JTAG mode select		N/C	
SCL	C30	System mgmt I2C serial clock	SCL_EEPROM	I2C SCL for EEPROM per FMC spec	3.3V, In/Out
SDA	C31	System mgmt I2C serial data	SDA_EEPROM	I2C SDA for EEPROM per FMC spec	3.3V, In/Out
GA0	C34	Geographical address bit 0 for EEPROM	GA0	Geographical address bit 0 for EEPROM (pulled high, EEPROM address = 0x53)	3.3V, In
GA1	C35	Geographical address bit 1 for EEPROM	GA1	Geographical address bit 1 for EEPROM (pulled high, EEPROM address = 0x53)	3.3V, In
VREF_A_M2C	H1	Reference voltage for voltage signaling		N/C	
VREF_B_M2C	K1	Reference voltage for signaling		N/C	
VIO_B_M2C1	J39	Voltage generated from mezzanine card to power IO bank B on FPGA		Tied to Vadj	DC, In

VIO_B_M2C0	K40	Voltage generated from mezzanine card to power IO bank B on FPGA		Tied to Vadj	DC, In
GBTCLK1_M2C_N	B21	Diff pair clock reference for DP data signals		N/C	
GBTCLK1_M2C_P	B20	Diff pair clock reference for DP data signals		N/C	
GBTCLK0_M2C_N	D5	Diff pair clock reference for DP data signals	FPGA_GBTCLK_N	FPGA global clock -	LVDS, Out
GBTCLK0_M2C_P	D4	Diff pair clock reference for DP data signals	FPGA_GBTCLK_P	FPGA global clock +	LVDS, Out
CLK1_C2M_N	J3	Diff pair clock driven from host to mezzanine card		N/C	
CLK1_C2M_P	J2	Diff pair clock driven from host to mezzanine card		N/C	
CLK1_M2C_N	K5	Diff pair clock driven from mezzanine card to host		N/C	
CLK1_M2C_P	K4	Diff pair clock driven from mezzanine card to host		N/C	
CLK0_C2M_N	G3	Diff pair clock driven from host to mezzanine card		N/C	
CLK0_C2M_P	G2	Diff pair clock driven from host to mezzanine card		N/C	
CLK0_M2C_N	H5	Diff pair clock driven from mezzanine card to host	FPGA_REF_CLK_N	FPGA reference clock -, AC coupled	LVDS, Out
CLK0_M2C_P	H4	Diff pair clock driven from mezzanine card to host	FPGA_REF_CLK_P	FPGA reference clock +, AC coupled	LVDS, Out
3P3VAUX	D32	3.3V auxiliary supply	3P3V_AUX	Auxiliary 3.3V supply; used only to power EEPROM per spec	DC, In
VADJ3	H40	Adjustable voltage level power from carrier to mezzanine	Vadj	Vadj supply set by carrier card (1.8V to 2.5V)	DC, In
VADJ2	G39	Adjustable voltage level power from carrier to mezzanine	Vadj	Vadj supply set by carrier card (1.8V to 2.5V)	DC, In
VADJ1	F40	Adjustable voltage level power from carrier to mezzanine	Vadj	Vadj supply set by carrier card (1.8V to 2.5V)	DC, In
VADJ0	E39	Adjustable voltage level power from carrier to mezzanine	Vadj	Vadj supply set by carrier card (1.8V to 2.5V)	DC, In
12P0V1	C37	Main 12V power input		N/C	

12P0V0	C35	Main 12V power input		N/C	
3P3V3	C39	Main 3.3V power input	3P3V	Main 3.3V supply for card	DC, In
3P3V2	D40	Main 3.3V power input	3P3V	Main 3.3V supply for card	DC, In
3P3V1	D38	Main 3.3V power input	3P3V	Main 3.3V supply for card	DC, In
3P3V0	D36	Main 3.3V power input	3P3V	Main 3.3V supply for card	DC, In
RES1	B1	Reserved		N/C	
PRSNT_M2C_L	H2	Module present signal – grounded	GND	N/C	
PG_C2M	D1	Power good for carrier, asserts high by carrier when Vadj, 12P0V, and 3P3V are within spec	PG_C2M		In
PG_M2C	F1	Power good mezzanine. Asserts high by the mezzanine card when VIO_B_M2C, VREF_A_M2C, and VREF_B_M2C are within spec.	FMC_MYK_PG	Asserts high when all power supplies are within tolerance	3.3V, Out
RES	B40	Reserved, unconnected.		N/C	
LA00_P_CC	G6	User defined signal on Bank A, clock capable		N/C	
LA00_N_CC	G7	User defined signal on Bank A, clock capable		N/C	
LA01_P_CC	D8	User defined signal on Bank A, clock capable		N/C	
LA01_N_CC	D9	User defined signal on Bank A, clock capable		N/C	
LA02_P	H7	User defined signal on Bank A	LED_RED	Turns on red LED	Vadj, In
LA02_N	H8	User defined signal on Bank A••••••••••••••	LED_GREEN	Turns on green LED	Vadj, In
LA03_P	G9	User defined signal on Bank A	LED_BLUE	Turns on blue LED	Vadj, In
LA03_N	G10	User defined signal on Bank A	FMC_SDA	I2C serial data line	Vadj, In/Out
LA04_P	H10	User defined signal on Bank A	FMC_AD9528_CS_N	AD9528 SPI chip select	Vadj, In
LA04_N	H11	User defined signal on Bank A		N/C	

LA05_P	D11	User defined signal on Bank A	FMC_SCL	I2C serial clock line	Vadj, In
LA05_N	D12	User defined signal on Bank A	FMC_SYSREF_REQ	AD9528 system reference request	Vadj, In
LA06_P	C10	User defined signal on Bank A	FMC_10M_EN	Internal 10 MHz enable (hi=enable, low=use external 10 MHz)	Vadj, In
LA06_N	C12	User defined signal on Bank A	FMC_SYSREF_REQ	AD9528 system reference request	Vadj, In
LA07_P	H13	User defined signal on Bank A		N/C	
LA07_N	H14	User defined signal on Bank A	AD9528_SPI_RESET_N	AD9528 SPI reset	Vadj, In
LA08_P	G12	User defined signal on Bank A		N/C	
LA08_N	G13	User defined signal on Bank A		N/C	
LA09_P	D14	User defined signal on Bank A	RX_SYNCB_P	LVDS sync signal associated with Rx channel data on the JESD204b interface	LVDS, In
LA09_N	D15	User defined signal on Bank A	RX_SYNCB_N	LVDS sync signal associated with Rx channel data on the JESD204b interface LVDS, In	
LA10_P	C14	User defined signal on Bank A	SNRX_SYNCB_P	LVDS sync signal associated with ObsRx channel data on the JESD204b interface	LVDS, In
LA10_N	C15	User defined signal on Bank A	SNRX_SYNCB_N	LVDS sync signal associated with ObsRx channel data on the JESD204b interface	LVDS, In
LA11_P	H16	User defined signal on Bank A	AD9528_SYSREF_IN_P	External SYSREF input clock	LVDS, In
LA11_N	H17	User defined signal on Bank A	AD9528_SYSREF_IN_N	External SYSREF input clock	LVDS, In
LA12_P	G15	User defined signal on Bank A	FMC_VCXO_153M6_EN	Enables the 153.6 MHz reference VCXO (high=153.6 MHz VCXO enabled, low=100 MHz VCXO enabled)	Vadj, In

LA12_N	G16	User defined signal on Bank A		N/C	
LA13_P	D17	User defined signal on Bank A	FMC_REF_SEL	Selects internal 10 or external 10 MHz reference to AD9528 (low=internal 10 MHz, high=external 10 MHz)	Vadj, Out
LA13_N	D18	User defined signal on Bank A		N/C	
LA14_N	C19	User defined signal on Bank A		N/C	
LA15_P	H19	User defined signal on Bank A	TX_SYNCB_P	LVDS sync signal associated with Tx channel data on the JESD204b interface	LVDS, Out
LA15_N	H20	User defined signal on Bank A	TX_SYNCB_N	LVDS sync signal associated with Tx channel data on the JESD204b interface	LVDS, Out
LA16_P	G18	User defined signal on Bank A		N/C	
LA16_P	G19	User defined signal on Bank A		N/C	
LA17_P_CC	D20	User defined signal on Bank A, clock capable	FPGA_AUX_CLK_P	Auxiliary clock from the AD9528, AC coupled	LVDS, Out
LA17_N_CC	D21	User defined signal on Bank A, clock capable	FPGA_AUX_CLK_N	Auxiliary clock from the AD9528, AC coupled	LVDS, Out
LA18_P	C22	User defined signal on Bank A	FPGA_SYSREF_P	FPGA SYSREF clock from AD9528	LVDS, Out
LA18_N	C23	User defined signal on Bank A	FPGA_SYSREF_N	FPGA SYSREF clock from AD9528	LVDS, Out
LA19_P	H22	User defined signal on Bank A	FMC_EN_RXA1	Enables the Rx1 front end LNAs	Vadj, In
LA19_N	H23	User defined signal on Bank A	FMC_EN_RXA2	Enables the Rx2 front end LNAs	Vadj, In
LA20_P	G21	User defined signal on Bank A	FMC_EN_ORX	Enables the ObsRx front end LNAs	Vadj, In
LA20_N	G22	User defined signal on Bank A	FMC_EN_TX	Enables the Tx1 output amplifier	Vadj, In
LA21_P	H25	User defined signal on Bank A		N/C	
LA21_N	H26	User defined signal on Bank A		N/C	
LA22_P	G24	User defined signal on Bank A	FMC_PLL1_RESET_N	RF front end SPI reset for Rx1 and Rx2	Vadj, In

LA22_N	G25	User defined signal on Bank A	FMC_PLL2_RESET_N	RF front end SPI reset for ObsRx and Tx1	Vadj, In
LA23_P	D23	User defined signal on Bank A	RX1_ENABLE	Enables Rx channel 1 signal path in AD9371	Vadj, In
LA23_N	D24	User defined signal on Bank A	RX2_ENABLE	Enables Rx channel 2 signal path in AD9371	Vadj, In
LA24_P	H28	User defined signal on Bank A	TX1_ENABLE	Enables Tx channel 1 signal path in AD9371	Vadj, In
LA24_N	H29	User defined signal on Bank A	TX2_ENABLE	Enables Tx channel 2 signal path in AD9371	Vadj, In
LA25_P	G27	User defined signal on Bank A	MYK_RESET_N	AD9371 chip reset (active low)	Vadj, In
LA25_N	G28	User defined signal on Bank A	GP_INT	General purpose interrupt from AD9371	Vadj, Out
LA26_P	D26	User defined signal on Bank A	MYK_SPI_DIN	AD9371 + AD9528 SPI data in	Vadj, In
LA26_N	D27	User defined signal on Bank A	MYK_SPI_DOUT	AD9371 + AD9528 SPI data out	Vadj, Out
LA27_P	C26	User defined signal on Bank A	MYK_SPI_CLK	AD9371 + AD9528 SPI clock	Vadj, In
LA27_N	C27	User defined signal on Bank A	MYK_SPI_CS_N	AD9371 SPI chip select (active low)	Vadj, In
LA28_P	H31	User defined signal on Bank A	FMC_FE_MOSI	RF front end SPI data in	Vadj, In
LA28_N	H32	User defined signal on Bank A	FMC_FE_CLK	RF front end SPI clock	Vadj, In
LA29_P	G30	User defined signal on Bank A	FMC_RX1_ATT_LE	Rx1 attenuator SPI latch enable	Vadj, In
LA29_N	G31	User defined signal on Bank A	FMC_RX2_ATT_LE	Rx2 attenuator SPI latch enable	Vadj, In
LA30_P	H34	User defined signal on Bank A	FMC_ORX_ATT_LE	ObsRx attenuator SPI latch enable	Vadj, In
LA30_N	H35	User defined signal on Bank A		N/C	
LA31_P	G33	User defined signal on Bank A	FMC_PLL1_CS_N	RF front end SPI chip select for Rx1 and Rx2 (active low)	Vadj, In
LA31_N	G34	User defined signal on Bank A	FMC_PLL2_CS_N	RF front end SPI chip select for ObsRx and Tx1 (active low)	Vadj, In
LA32_P	H37	User defined signal on Bank A	FMC_MYK_PWR_EN	Enable AD9371 power supplies	Vadj, In
LA32_N	H38	User defined signal on Bank A		N/C	

LA33_N	G36	User defined signal on Bank A		N/C	
LA33_N	G37	User defined signal on Bank A		N/C	

Table 6: *FMC Low Pin Count Pinout*

FMC HIGH PIN COUNT (HPC) SECTION

FMC Signal Name	FMC Pin	FMC Description	Sidekiq X2 Net Name	Description	Logic Standard, I/O Type
DP0_C2M_P	C2	Gigabit interface diff pair driven from host to mezzanine	TX_SERD0_P	JESD204b input lane for Tx	CML, In
DP0_C2M_N	C3	Gigabit interface diff pair driven from host to mezzanine	TX_SERD0_N	JESD204b input lane for Tx	CML, In
DP1_C2M_P	A22	Gigabit interface diff pair driven from host to mezzanine	TX_SERD1_P	JESD204b input lane for Tx	CML, In
DP1_C2M_N	A23	Gigabit interface diff pair driven from host to mezzanine	TX_SERD1_N	JESD204b input lane for Tx	CML, In
DP2_C2M_P	A26	Gigabit interface diff pair driven from host to mezzanine	TX_SERD2_P	JESD204b input lane for Tx	CML, In
DP2_C2M_N	A27	Gigabit interface diff pair driven from host to mezzanine	TX_SERD2_N	JESD204b input lane for Tx	CML, In
DP3_C2M_P	A30	Gigabit interface diff pair driven from host to mezzanine	TX_SERD3_P	JESD204b input lane for Tx	CML, In
DP3_C2M_N	A31	Gigabit interface diff pair driven from host to mezzanine	TX_SERD3_N	JESD204b input lane for Tx	CML, In
DP4_C2M_P	A34	Gigabit interface diff pair driven from host to mezzanine		N/C	
DP4_C2M_N	A35	Gigabit interface diff pair driven from host to mezzanine		N/C	
DP5_C2M_P	A38	Gigabit interface diff pair driven from host to mezzanine		N/C	
DP5_C2M_N	A39	Gigabit interface diff pair driven from host to mezzanine		N/C	
DP6_C2M_P	B36	Gigabit interface diff pair driven from host to mezzanine		N/C	
DP6_C2M_N	B37	Gigabit interface diff pair driven from host to mezzanine		N/C	

DP7_C2M_P	B32	Gigabit interface diff pair driven from host to mezzanine		N/C	
DP7_C2M_N	B33	Gigabit interface diff pair driven from host to mezzanine		N/C	
DP8_C2M_P	B28	Gigabit interface diff pair driven from host to mezzanine		N/C	
DP8_C2M_N	B29	Gigabit interface diff pair driven from host to mezzanine		N/C	
DP9_C2M_P	B24	Gigabit interface diff pair driven from host to mezzanine		N/C	
DP9_C2M_N	B25	Gigabit interface diff pair driven from host to mezzanine		N/C	
DP0_M2C_P	C6	Gigabit interface diff pair driven from mezzanine to host	RX_SERD0_P	JESD204b output lane for Rx	CML, Out
DP0_M2C_N	C7	Gigabit interface diff pair driven from mezzanine to host	RX_SERD0_N	JESD204b output lane for Rx	CML, Out
DP1_M2C_P	A2	Gigabit interface diff pair driven from mezzanine to host	RX_SERD1_P	JESD204b output lane for Rx	CML, Out
DP1_M2C_N	A3	Gigabit interface diff pair driven from mezzanine to host	RX_SERD1_N	JESD204b output lane for Rx	CML, Out
DP2_M2C_P	A6	Gigabit interface diff pair driven from mezzanine to host	RX_SERD2_P	JESD204b output lane for Rx	CML, Out
DP2_M2C_N	A7	Gigabit interface diff pair driven from mezzanine to host	RX_SERD2_N	JESD204b output lane for Rx	CML, Out
DP3_M2C_P	A10	Gigabit interface diff pair driven from mezzanine to host	RX_SERD3_P	JESD204b output lane for Rx	CML, Out
DP3_M2C_N	A11	Gigabit interface diff pair driven from mezzanine to host	RX_SERD3_N	JESD204b output lane for Rx	CML, Out
DP4_M2C_P	A14	Gigabit interface diff pair driven from mezzanine to host		N/C	
DP4_M2C_N	A15	Gigabit interface diff pair driven from mezzanine to host		N/C	
DP5_M2C_P	A18	Gigabit interface diff pair driven from mezzanine to host		N/C	
DP5_M2C_N	A19	Gigabit interface diff pair driven from mezzanine to host		N/C	
DP6_M2C_P	B16	Gigabit interface diff pair driven from mezzanine to host		N/C	
DP6_M2C_N	B17	Gigabit interface diff pair driven from mezzanine to host		N/C	
DP7_M2C_P	B12	Gigabit interface diff pair driven from mezzanine to host		N/C	

DP7_M2C_N	B13	Gigabit interface diff pair driven from mezzanine to host		N/C	
DP8_M2C_P	B8	Gigabit interface diff pair driven from mezzanine to host		N/C	
DP8_M2C_N	B9	Gigabit interface diff pair driven from mezzanine to host		N/C	
DP9_M2C_P	B4	Gigabit interface diff pair driven from mezzanine to host		N/C	
DP9_M2C_N	B5	Gigabit interface diff pair driven from mezzanine to host		N/C	
HA00_P_CC	F4	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C (clock capable)	MYK_GPIO0	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA00_N_CC	F5	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C (clock capable)	MYK_GPIO1	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA01_P_CC	E2	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C (clock capable)	MYK_GPIO2	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA01_N_CC	E3	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C (clock capable)	MYK_GPIO3	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA02_P	K7	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C	MYK_GPIO4	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA02_N	K8	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C	MYK_GPIO5	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA03_P	J6	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA03_N	J7	User defined signal on Bank A, uses reference voltage on pin VREFAM2C		N/C	
HA04_P	F7	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C	MYK_GPIO6	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA04_N	F8	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C	MYK_GPIO7	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA05_P	E6	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C	MYK_GPIO8	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA05_N	E7	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C	MYK_GPIO15	AD9371 GPIO referenced to Vadj	Vadj, In/Out

HA06_P	K10	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C	MYK_GPIO9	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA06_N	K11	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C	MYK_GPIO10	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA07_P	J9	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA07_N	J10	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA08_P	F10	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C	MYK_GPIO11	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA08_N	F11	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C	MYK_GPIO12	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA09_P	E9	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA09_N	E10	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C	MYK_GPIO18	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA10_P	K13	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA10_P	K14	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA11_P	J12	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA11_P	J13	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA12_P	F13	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA12_N	F14	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA13_P	E12	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C	MYK_GPIO13	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA13_N	E13	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C	MYK_GPIO14	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA14_P	J15	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C			
HA14_N	J16	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C			
HA15_P	F16	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C			
HA15_N	F17	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C			
HA16_P	E15	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C	MYK_GPIO16	AD9371 GPIO referenced to Vadj	Vadj, In/Out

HA16_N	E16	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C	MYK_GPIO17	AD9371 GPIO referenced to Vadj	Vadj, In/Out
HA17_P_CC	K16	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C (clock capable)		N/C	
HA17_P_CC	K17	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C (clock capable)		N/C	
HA18_P	J18	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA18_N	J19	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA19_P	F19	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA19_N	F20	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA20_P	E18	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA20_N	E19	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA21_P	K19	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA21_N	K20	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA22_P	J21	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA22_N	J22	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA23_P	K22	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HA23_N	K23	User defined signal on Bank A, uses reference voltage on pin VREF_A_M2C		N/C	
HB00_P_CC	K25	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C (clock capable)		N/C	
HB00_N_CC	K26	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C (clock capable)		N/C	
HB01_P	J24	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB01_N	J25	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB02_P	F22	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	

HB02_N	F23	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB03_P	E21	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB03_N	E22	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB04_P	F25	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB04_N	F26	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB05_P	E24	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB05_N	E25	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB06_P	K28	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB06_N	K29	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB07_P	J27	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB07_N	J28	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB08_P	F28	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB08_N	F29	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB09_P	E27	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB09_N	E28	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB10_P	K31	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB10_N	K32	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB11_P	J30	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB11_N	J31	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB12_P	F31	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB12_N	F32	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB13_P	E30	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB13_N	E31	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB14_P	K34	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB14_N	K35	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB15_P	J33	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB15_N	J34	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB16_P	F34	User defined signal on Bank A, uses reference voltage on pin VREF*B*M2C		N/C	
HB16_N	F35	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB17_P_CC	K37	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB17_N_CC	K38	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB18_P	J36	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	

HB18_N	J37	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB19_P	E33	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB19_N	E34	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB20_P	F37	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB20_N	F38	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	
HB21_P	E36	User defined signal on Bank A, uses reference voltage on pin VREF*B*M2C		N/C	
HB21_N	E37	User defined signal on Bank A, uses reference voltage on pin VREF_B_M2C		N/C	

Table 7: *FMC High Pin Count Pinout*

BASIC USAGE IN A HOST SYSTEM

HOST SYSTEM COMPATIBILITY

Sidekiq X2 is expected to be deployed into a host system that adheres to a general architecture in order to utilize the core FPGA reference design and associated libsidekiq software API. This general architecture is shown in Figure 5 below.

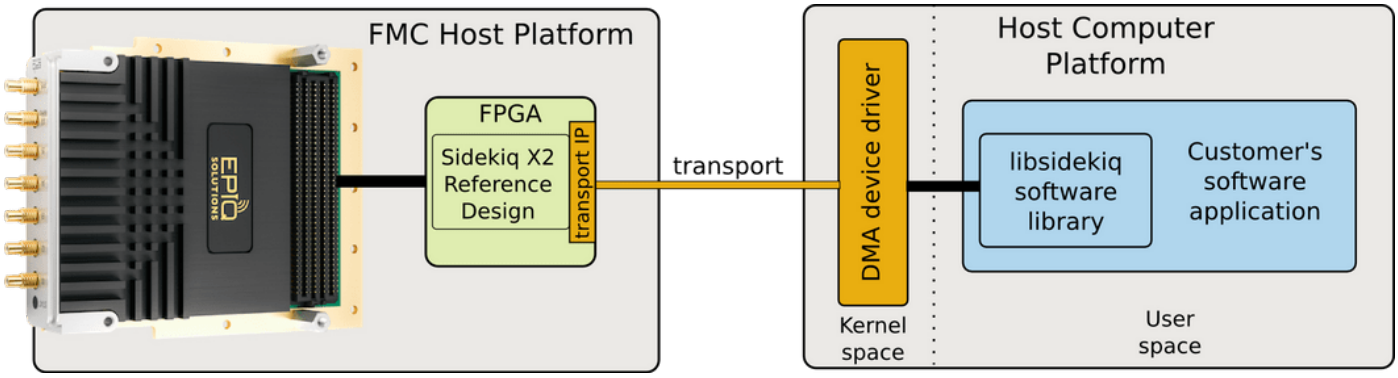


Figure 5: *General Sidekiq X2 deployment architecture*

A typical deployment scenario into a host platform is shown in Figure 6, which depicts the Sidekiq X2 plugged into a COTS PCIe FPGA board (HiTech Global's HTG-K800 [5]), mounted into a Thunderbolt 3 chassis, connected to a host computer running Linux through a Thunderbolt 3 cable. In this deployment, the FPGA on the HTG-K800 is the Xilinx Kintex Ultrascale XCKU060, and a Gen3 x4 PCIe interface native to the FPGA is utilized to provide the transport between the FPGA and host computer via the Thunderbolt 3 chassis. On the host computer, a Linux device driver supports both PCIe register reads/writes as well as DMA between the FPGA and the CPU in the host computer. The libsidekiq API then uses PCIe as the transport layer to support all of the standard Sidekiq API calls.

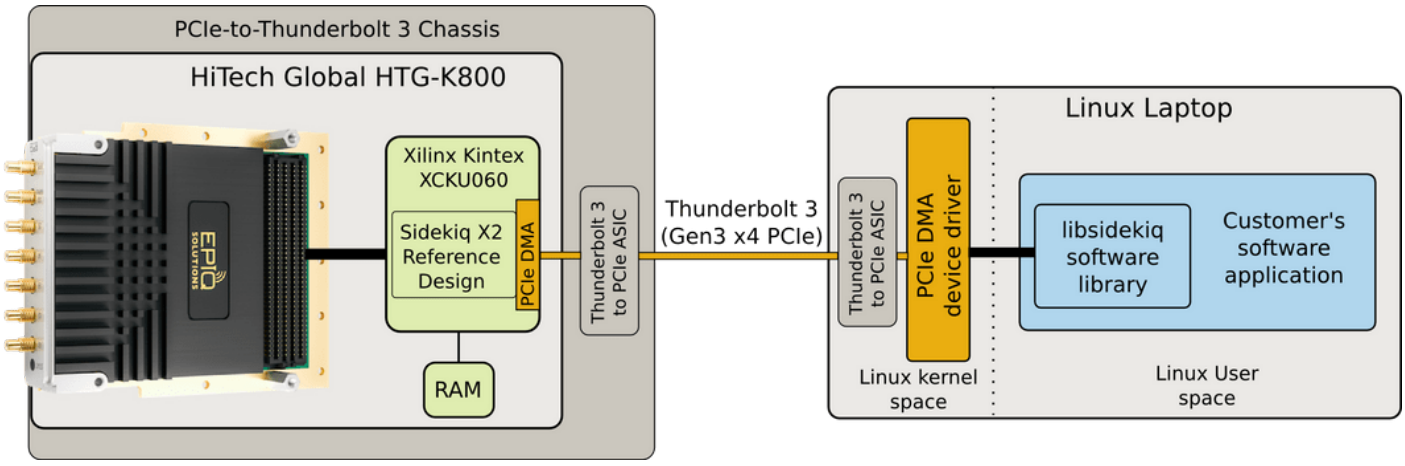


Figure 6: *Sidekiq X2 deployment architecture with PCIe carrier, Thunderbolt 3 chassis, and a host Linux PC*

In an alternate deployment scenario, Sidekiq X2 can be interfaced to a 3U VPX carrier card that hosts an integrated FPGA + CPU in a single chip, such as the Xilinx Zynq Ultrascale+ SoC. In this scenario, both the FPGA fabric required to execute the Sidekiq X2 FPGA reference design and the multi-core ARM CPU running the libsidekiq software library are located on a single device (i.e., the Zynq Ultrascale+ SoC). The transport layer used to interface between the Zynq's FPGA fabric (PL) and the Zynq's ARM CPU (PS) is an efficient AXI-based DMA interconnect. This is shown in Figure 7 below.

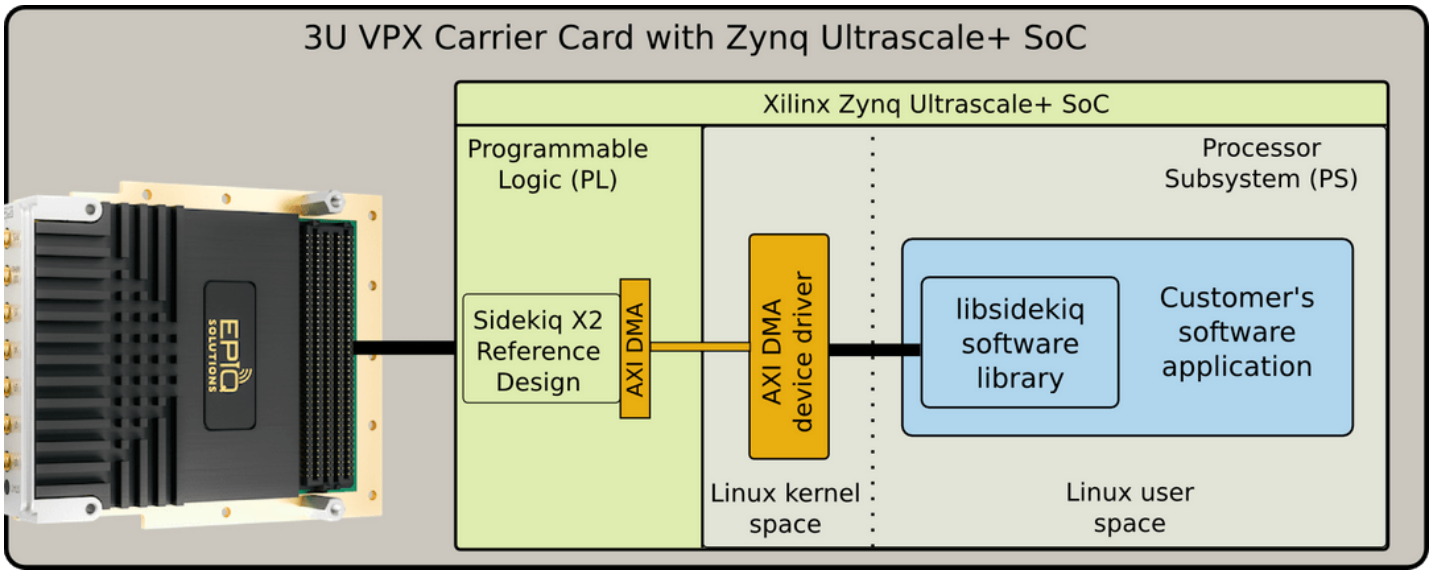


Figure 7: *Sidekiq X2 deployment architecture with a Zynq Ultrascale+ SoC*

Note that this configuration with the Zynq Ultrascale+ SoC in a 3U VPX platform could also use PCIe as the transport to interface to the VPX backplane. In this configuration, the AXI transport is no longer needed, and all transport activities would be targeting a 3U VPX computer card plugged into the 3U VPX backplane, similar to the architecture shown in Figure 6.

OPERATING SYSTEM COMPATIBILITY

Linux is the only operating system that is currently supported. Various kernel versions have been tested starting at Linux version 3.0. Sidekiq has been tested both in x86-based Linux systems as well as ARM-based Linux systems. Kernel versions prior to 3.0 (i.e., 2.6+) may also be supported.

For customers interested in doing a custom build of the Sidekiq PCIe device driver for their host platform, a license for the source code for this device driver is also available separately. Please contact Epiq Solutions for details.

Alternate operating systems, such as Windows, may also be supported in the future. Please contact Epiq Solutions for details.

POWER CONSUMPTION

The power consumption of Sidekiq X2 card is largely dependent on the number of RF channels being utilized and the sample rate at which those channels are operating. The power consumption of the card will vary between ~4W and ~10W based on this configuration. A table showing several example use cases is shown below. For each of these cases, the power consumption of the X2 card is measured by performing a DC current measurement on the 3.3V power rail provided by the FMC interface. This is the only power rail required by the X2 card for operation.

Test Scenario	Power Consumption (in Watts)
Test scenario #1:	6.7
Test scenario #2:	6.5
Test scenario #3:	6.6
Test scenario #4:	6.3

Table 8: *Example power consumption measurements for Sidekiq X2*

THERMAL DISSIPATION

Effective use of Sidekiq X2 in a system also requires consideration of an appropriate thermal dissipation solution. Sidekiq X2 can be integrated into a variety of different host systems with different thermal profiles (i.e., forced air, natural convection, etc), and the end user is required to perform their own system analysis to determine what level of thermal dissipation is appropriate for their use-case. For a standard convection cooled deployment, the required air flow over the heatsink on the card is TBD LFM. Sidekiq X2 uses components that are rated for operation to +85 deg C, and thus the end user must ensure that the temperature reported by the on-board temperature sensor does not exceed +85 deg C. The on-board temperature of the card can be queried through a temperature sensor, which can then be reported up to the host software application via the libsidekiq API. **Exceeding the maximum rated temperature of +85 deg C may damage the Sidekiq X2 card and/or accelerate failure of the card.**

The following are the key circuit elements dissipating power on Sidekiq X2. The listed power values represent **worst case** at 100% duty cycle; actual power dissipation will be application dependent.

IC	Part Number	Reference	Pdiss	Side
RFIC	AD9371	U11	6 W	Top
Clock Distribution	AD9528	U9	1.4W	Bottom
Up/down converters	RFFC5071	U17, U19	0.6W each	Bottom
Voltage regulators	ADP2114	U41, U42	0.25W each	Bottom

Table 9: *Sidekiq X2 component power consumption*

The side with the FMC connector is designated "Top". Component locations are shown below.

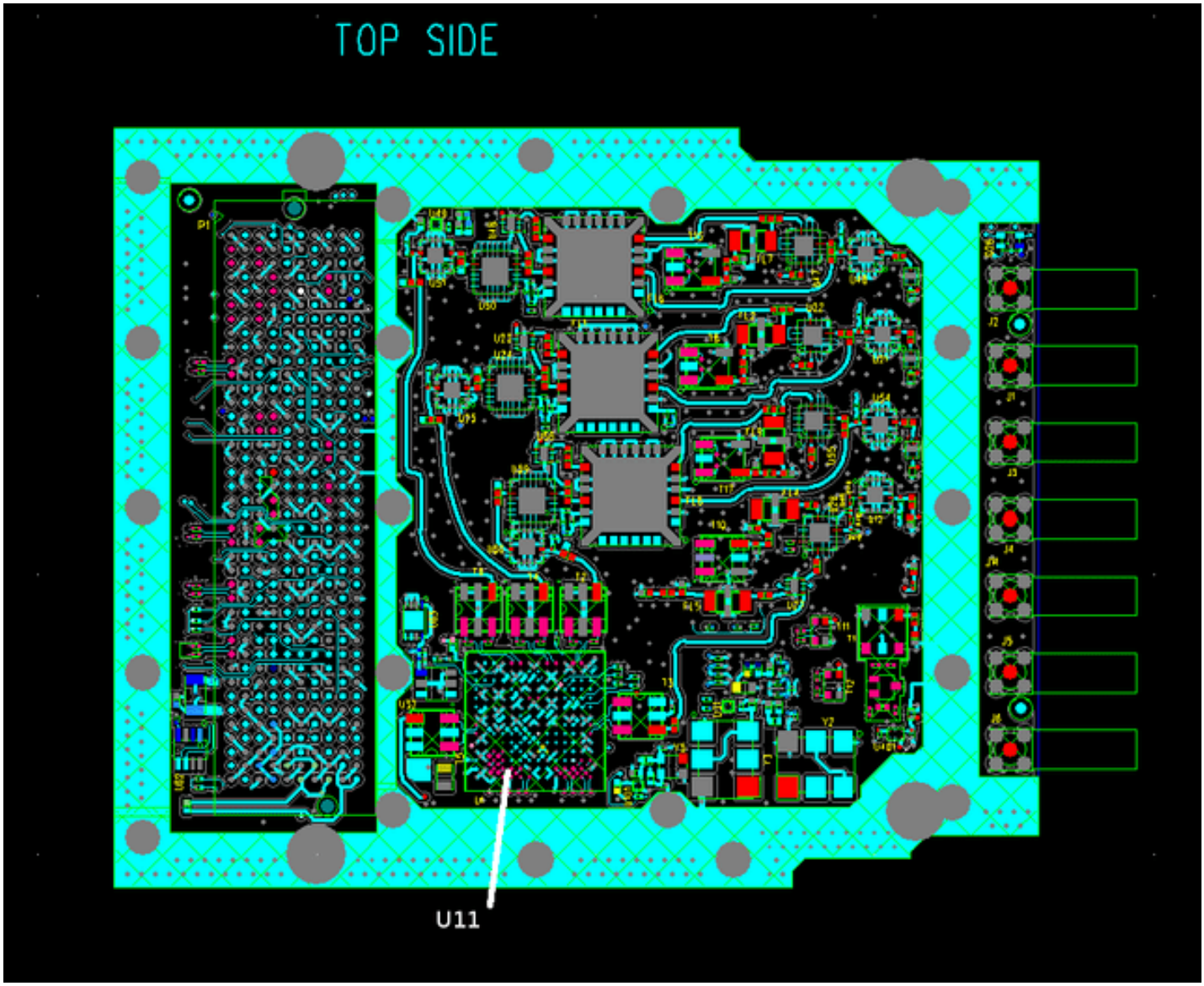


Figure 8: *Sidekiq X2 Top*

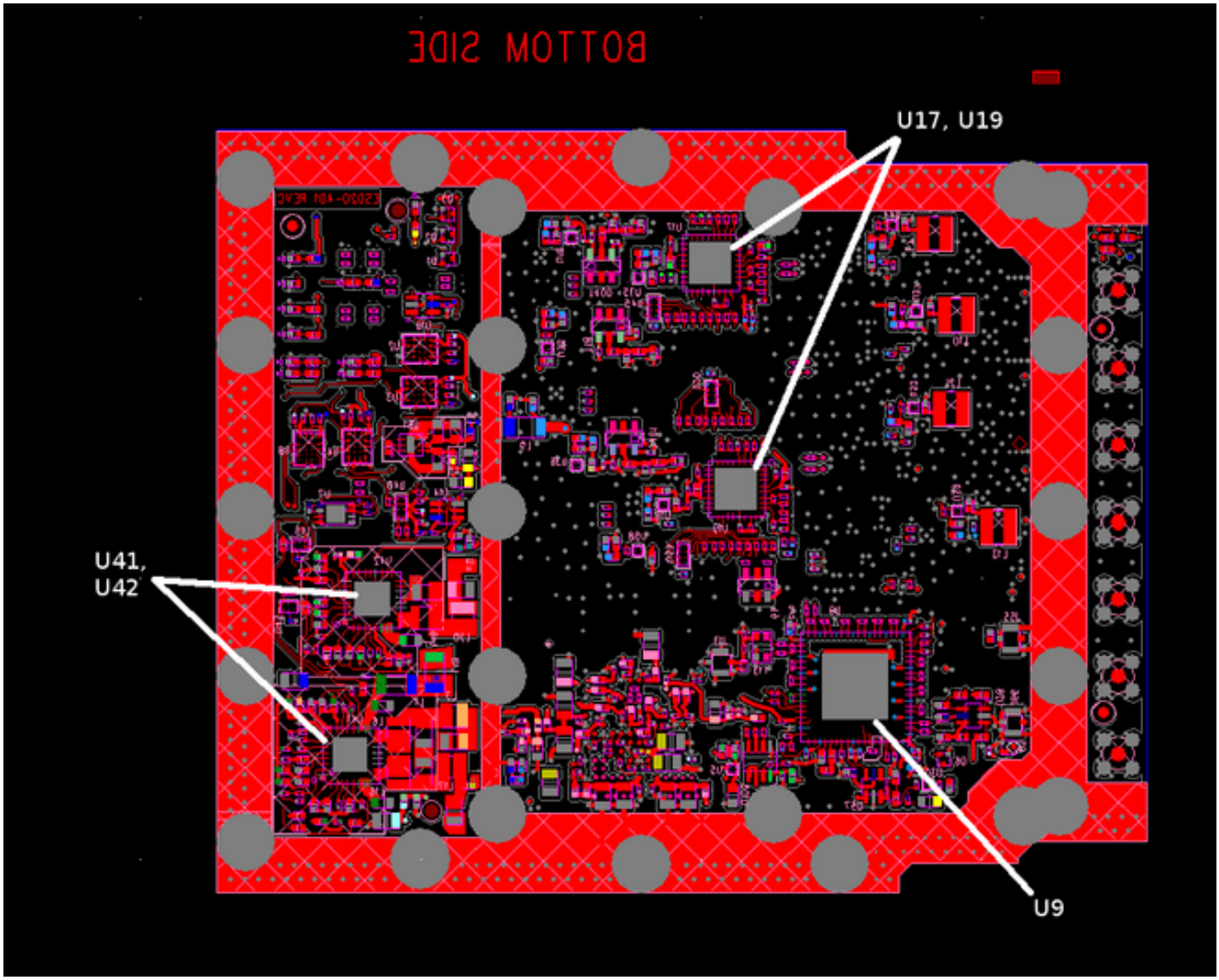


Figure 9: *Sidekiq X2 Bottom*

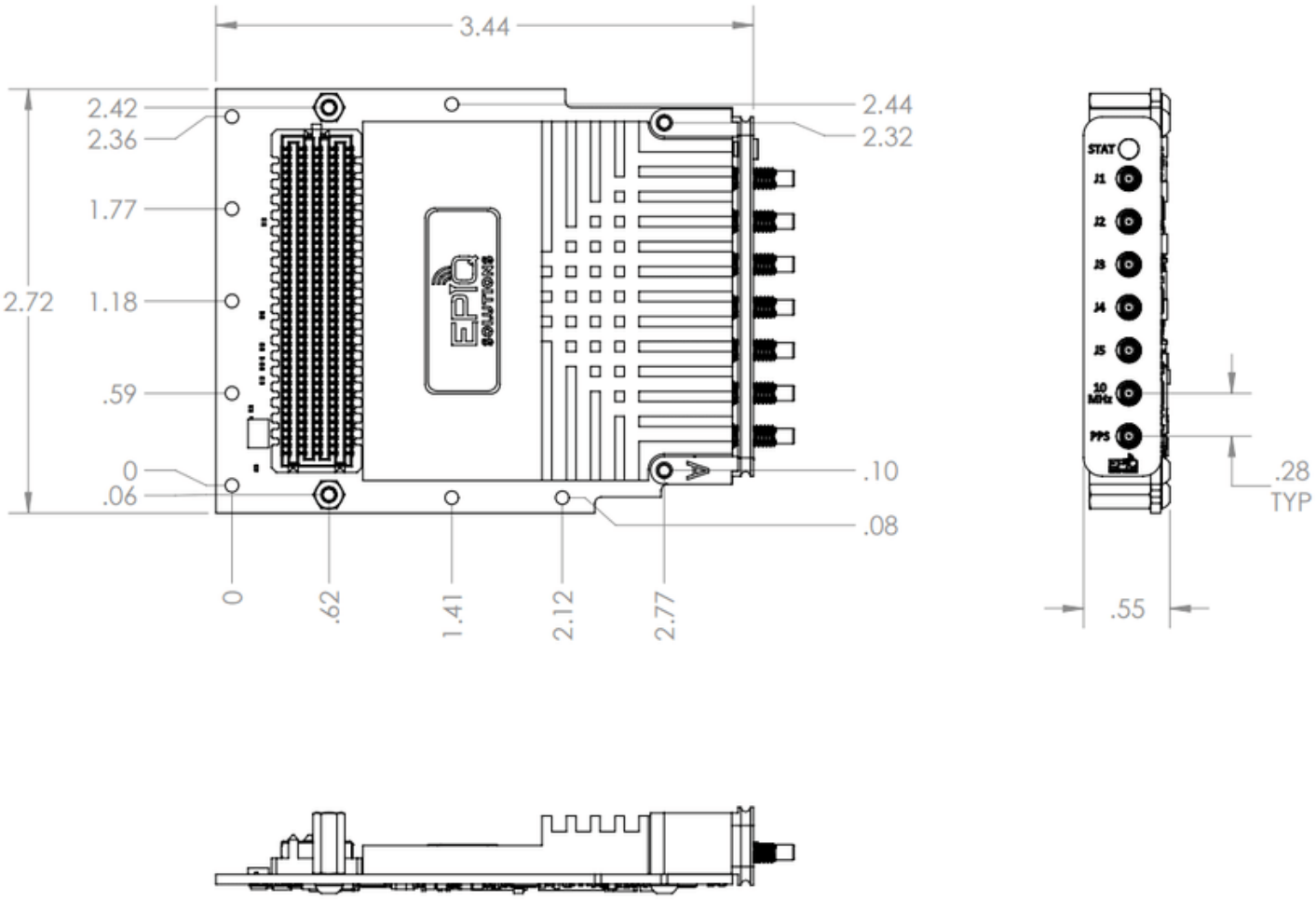
- The thermal gap pad material used on the X2 RFIC (U11) is Bergquist Gap Pad P/N: GPVOUS-0.040-00
- The thermal pad is 0.472" x 0.472" x 0.040" thick and is compressed around 50%.
- For air-cooled designs, the heat is primarily conducted directly away from the top surfaces of the RFICs as delivered with the heat sink/shield. The heat sink/shield is secured to the perimeter exposed metal with screws which does also provide some conduction to the heat sink.

JTAG ACCESS ON SIDEKIQ

The standard FMC interface includes pins for addressing JTAG devices local to the card. On Sidekiq X2, there are no devices on the JTAG chain. The TDI line is directly connected to the TDO line to allow the JTAG chain to pass through the FMC interface.

SIDEKIQ X2 MECHANICAL OUTLINE

A dimensioned mechanical drawing of Sidekiq X2 in convection cooled form is shown in Figure 9. In addition, a 3D model (in STP format) is also available. Please contact Epiq Solutions for this model.



Conduction cooled variants of Sidekiq X2 are also supported, which require an alternate heatframe for cooling as well as a replacement of the front panel SSMC connectors with footprint compatible MMCX or SMP connectors. Please contact Epiq Solutions for details.

SIDEKIQ X2 THUNDERBOLT 3 PLATFORM

OVERVIEW

The Sidekiq X2 Platform Development Kit (PDK) includes one Sidekiq X2 card integrated on to a COTS FPGA PCIe card (Hi Tech Global HTG-K800 [5]) with a Xilinx Kintex Ultrascale XCKU060 FPGA. This PCIe card is then installed in to a COTS Thunderbolt 3 chassis that converts the Gen3 x4 PCIe interface available on the HTG-K800 into Thunderbolt 3, and presents this interface through the Thunderbolt 3 interface accessible on the chassis. A Thunderbolt 3 cable can then connect the chassis to a Linux host PC, where the system appears as a PCIe device plugged into the system. A picture of Sidekiq X2 + HTG-K800 PCIe card installed into the Thunderbolt 3 chassis and connected to a host laptop is shown in Figure 9.

Figure 10: *Sidekiq X2 + HTG-K800 FPGA host board installed into a Thunderbolt 3 chassis, interfaced to a laptop via a Thunderbolt 3 cable*

BASIC USAGE THE SIDEKIQ X2 THUNDERBOLT 3 PLATFORM

The following steps can be followed to perform a basic RF recording (using the rx_samples test application) and RF playback (using the tx_samples test application) with the Sidekiq X2 Thunderbolt 3 platform that ships with the PDK:

Step 1. With the Sidekiq X2 Thunderbolt 3 platform powered on *first* (using the provided DC power brick for the Thunderbolt 3 chassis), connect the TB3 chassis to the laptop with the provided TB3 cable and power on the laptop *last*. The TB3 chassis will fully power-on when the laptop is connected and powered-up.

Step 2. Log into Ubuntu laptop with the user credentials:

Username: **sidekiq**

Password: **sidekiq**

Step 3. Launch a terminal window or by pressing Ctrl-Alt-T.

Step 4. Navigate to */home/sidekiq/sidekiq_image_current/test_apps/*

Step 5. A user can perform an RF recording of I/Q samples using the default configuration by executing the *rx_samples* application as follows:

```
./rx_samples -d <FILE>
```

This command will save I/Q samples to a file named <FILE>.a1 using default values for RF frequency, sample rate, and other parameters. The data is stored in the file as 16-bit I/Q pairs with 'I' samples stored in the upper 16-bits of each word, and 'Q' samples stored in the lower 16-bits of each word. Additional available options are described by executing:

```
./rx_samples -h
```

Configuration of frequency, sample rate, bandwidth, number of samples, and more are available with additional command line parameters.

Step 6. A file of I/Q samples can also be transmitted out by running the *tx_samples* application using the default configuration as follows:

```
./tx_samples -s <FILE>
```

This application expects the same I/Q file format for samples as produced by the rx_samples application. Additional available options are described by executing:

```
./tx_samples -h
```

Configuration of frequency, sample rate, bandwidth, timestamp modes, block size, and more are available with additional command line parameters. It is highly recommended that a user profile their system for an adequate transmit block and mode configuration by running tx_benchmark (more details in the Sidekiq SDK Manual, Appendix 8 - Assessing Throughput Performance)

Both rx_samples and tx_samples are test applications to serve as examples of how to use the libsidekiq API. The source code for these test applications and others are distributed with the SDK at /home/sidekiq/sidekiq_sdk_vX, where 'X' represents the version of the release.

ACCESSING JTAG ON THE SIDEKIQ X2 THUNDERBOLT 3 PLATFORM

For customers adding their own custom FPGA blocks in the "user_app" area of the Sidekiq X2 reference design, it can often be useful to access JTAG to monitor signals in the FPGA through Xilinx's Chipscope software running on a separate PC. The HTG-K800 FPGA PCIe card provides access to the JTAG port of the XCKU060 FPGA through a 2x7 header on the top side of the board. A standard Xilinx JTAG USB platform cable, such as the HW-USB-II-G, can be utilized to access JTAG on the FPGA. In order to access this JTAG header, the Thunderbolt 3 platform must first be powered down, and the outer shell of the Thunderbolt 3 chassis must be removed by unscrewing the two front thumbscrews and carefully sliding the internal board stack out. Once the shell is removed, the JTAG header is accessible, as shown in Figure 10 below. **Note: it is critical that the user exercise proper electrical safety measures and ESD protection when interacting with open frame electronics. Failure to do so can permanently damage both the Sidekiq X2 card as well as the HTG-K800 FPGA board.**

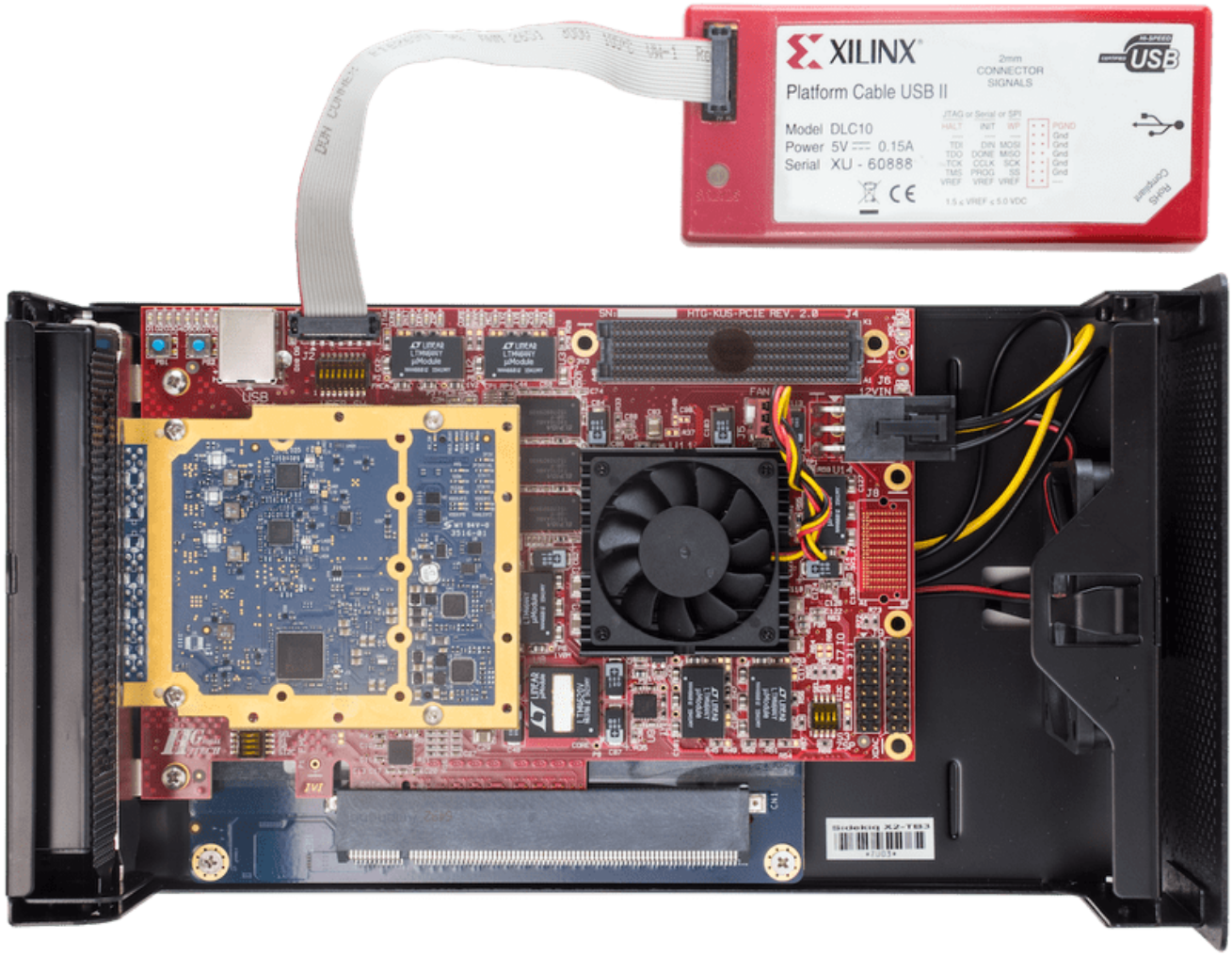


Figure 11: *JTAG port access on the Sidekiq X2 Thunderbolt 3 platform*

Once the JTAG cable is installed, the Thunderbolt 3 chassis cover can be carefully replaced, as shown in Figure 11, with the JTAG cable coming through the front panel of the unit. This ensures that the airflow from the internal fans is properly ducted over the critical components including Sidekiq X2.

Figure 12: *Thunderbolt 3 chassis closed up with Xilinx JTAG interface installed*

With the Thunderbolt 3 chassis reassembled, the user can resume normal usage of the system.

APPENDIX A - SIDEKIQ X2 STATEMENT OF VOLATILITY

Model	Sidekiq X2
Part Number	ES020-104
Manufacturer	Epiq Solutions
Address	3740 Industrial Avenue Rolling Meadows, IL 60008

Table 10: *Model, Part Number, and Manufacturer Info*

Memory Type	Memory Size	User Modifiable	Removable	Purpose	Process to Clear
AD9528 Clock Generator	1.3 KB	Yes	No	Clock control registers	Power-off
AD9371	???	Yes	No	RFIC ARM memory and configuration space	Power-off

Table 11: *Sidekiq X2 Volatile Memory*

Memory Type	Memory Size	User Modifiable	Removable	Purpose	Process to Clear
EEPROM	2 Kbit	No	No	Holds product information for identifying FMC device (part#, serial#, and power requirements)	Must be returned to factory to clear
EEPROM	512 Kbit	Yes	No	Holds factory calibration data and user configuration settings: ref_clk selection	Factory calibration data is read-only and must be sent back to factory to clear. Ref_clk setting is read/write via API.

Table 12: *Sidekiq X2 Non-Volatile Memory*

APPENDIX B - FAILURE RATE & MTBF

Listed below is the Failure Rate and MTBF for the ES020-211-C Sidekiq X2 Assembly with Preselect Filters and SSMC RF Connectors.

The Calculations are derived from Relyence Reliability Software and based off a fixed/ground/controlled operating environment with an ambient temperature of 25°C.

Part Number	ES020-211-C
Description	Sidekiq X2 Assembly with Preselect Filters and SSMC RF Connectors
Failure Rate (fpmh)	0.688275
MTBF (hours)	1,452,908.03
Calculation Model	Telcordia Issue 4
Operating Environment	Fixed/Ground/Controlled
Ambient Temperature	25°C

Table 13: *Sidekiq X2 Failure Rate & MTBF*