Matchstiq™ V40

EARLY ACCESS

Direct-Sampling Multi-GHz Bandwidth SDR in a Low-SWaP Package

Complete 9 GHz SDR Platform including RF front-end, direct RF sampling, user-accessible FPGA, on-board processing and 100 GbE VITA 49 offload in a small robust package.

The Epiq Solutions Matchstiq V40 is a next generation, direct sampling software defined radio (SDR). It offers a compelling combination of flexibility, bandwidth, processing power, for applications where low Size, Weight and Power (SWaP) and superior RF performance are the priorities. It achieves this by combining the Analog Devices AD9084 MxFE RF front end with a carefully selected AMD Versal Adaptive SoC. Together they form a low-latency platform with up to 2 GHz instantaneous bandwidth, large numbers of definable digital down converters (DDCs) and digital up converters (DUCs), fast frequency hopping and an extremely fast sweep speed. The V40 supports three operational modes: Standalone with customer developed software applications and FPGA IP to enable advanced processing; as a 100 GbE VITA 49 streaming device; or a combination of both. Other features include dynamic reconfiguration, full bandwidth signal monitoring and snapshot memory.

Product Web Page:

Key Features

- 9 GHz direct sampling radio architecture
- 2 GHz of instantaneous bandwidth for processing on receive and transmit
- Single physical channels assignable to large numbers of Digital Down Converter/ Digital Up Converter channels within 2 GHz window
- Low latency digital architecture
- VITA 49 streaming on 100 GbE
- Low SWaP package (<50 inch^3 and 40 W power)
- Open architecture software environment

Specifications at a Glance

Category	Output	F_{Min}	F_{Max}	Frequency Tuning	Timing Inputs	CPU Enabled	GPU Enabled
Platform	Digital	1 MHz	9 GHz	Indep.	10 MHz, PPS, GPS	Yes	No

Max Rx Channels	Max Tx Channels	IBW_{Max}	$SFDR_{Typ.}$	Weight	Typ. Power Consumption	Interfaces	ADC bits/ DAC bits
1	1	2,000 MHz	70 dB	2.2 lb. 1 kg	40 W	100 GbE	12-16/ 16

Specifications

Model:	V40
Environmental Specifications	
Temperature (Operating)	-40 to +70 °C, cold plate surface temperature under typical operating conditions
Temperature (Storage)	-40 to +85 °C
Size	7.02 x 4.34 x 1.635 inches 178 x 110 x 42 mm
Weight	2.2 lb. 1.0 kg
Power (Typ.)	<40 W
Voltage Input Range	9-28 Vdc
Enclosure	Metal
Digital Specifications	
FPGA	Versal Adaptive SoC XCVM1302
CPU/ GPU	Dual ARM Cortex-A72 MPCore/ No GPU
Memory	4 GB DDR4 (PS), 4 GB DDR4 (PL)
Storage	128 GB eMMC, 128 MB QSPI Flash
User I/O	QSFP28 100 GbE for VITA 49 streaming to external GPU etc.
	USB-C maintenance access to serial console (UART)
	USB-C access to USB 3.0 host
	RJ45 1 GbE Network port for command and control
	microSD slot under removable cover. System capable of secure boot from suitable user-supplied card.
	GPIO access through front panel connector
	User accessible JTAG interface under removable cover
	Multi-color System LED
DDCs/ DUCs	Programmable channelization within up to 2 GHz of instantaneous bandwidth. 4 of each are predefined in the PDK as a starting point.
Other	
Export Classification	5A991.b
CE-Marked	-

Model:	V40	
RF Specifications		
All		
Connector Types	SMA Female	
Frequency Range	1 MHz to 9 GHz	
Sample Rate	2.5 GS/s, maximum contiguous payload, at 16 bits	
Channel Bandwidth	Up to 2 GHz	
Tuning Operation	Defined by NCOs (Numerically Controlled Oscillators)	
Snapshot Capture	Up to 4 GB of PL memory can be allocated between transmit and receive, with 2 GB each side by default. As an example, 2 GB allocated to Rx enables 200 ms of capture at the full 2 GHz IBW	
Receive		
Channels	1 Physical Channel	
Max RF Input Level	+20 dBm	
Tuning Time [1]	<1 µs	
Noise Figure (Typ.)	1 GHz 3 GHz 6 GHz 9 GHz	8 dB 9 dB 10 dB 12 dB
Input IP3 (Typ.) [2]	1 GHz 3 GHz 6 GHz 9 GHz	-2 dBm -2 dBm 0 dBm 0.5 dBm
Spurious Free Dynamic Range (Typ.) [3]	1 GHz 3 GHz 6 GHz 9 GHz	70 dBc 70 dBc 70 dBc 70 dBc
Internal Spurs [4]	1 GHz 3 GHz 6 GHz 9 GHz	-111 dBm -110 dBm -109 dBm -106 dBm

Continues...

[1] Tuning between any two frequencies over operating range

[2] Measured with 2 CW tones at -9 dB-full-scale of the A/D input power

[3] Highest in-band spur compared against a single CW tone at -9 dB-full-scale of the A/D

[4] Highest in-band spur translated to equivalent power at the Rx input connector

Specifications

Model:	V40
Receive Continued	
Max ADC Sample Rate	20 GS/s
A/D Bits	ADC samples at 20 GS/s with 12 bit, extendable to 16 bit through decimation and processing gain
Transmit	
Channels	1 Physical Channel
Typical Output Power	+5 dBm
Spurious Free Dynamic Range (Typ.) [5]	70 dB
Tuning Time [6]	<1 µs
Maximum DAC Sample Rate	28 GS/s
D/A Bits	16
Clocking	
Reference	10 MHz (MMCX Connector)
PPS Input	Yes (MMCX Connector)
GPS Input	Yes (50 Ω SMA) 3.3V, 50 mA antenna bias available

Data subject to change without notice.

(Antennas not included)

System Highlights

Direct Sampling, High Performance RF Front End

- 20 GS/s ADCs and 28 GS/s DACs
- RF Coverage from 1 MHz to 9 GHz
- Integrated RF Front End for Filtering & Amplification

Flexible Digital Architecture

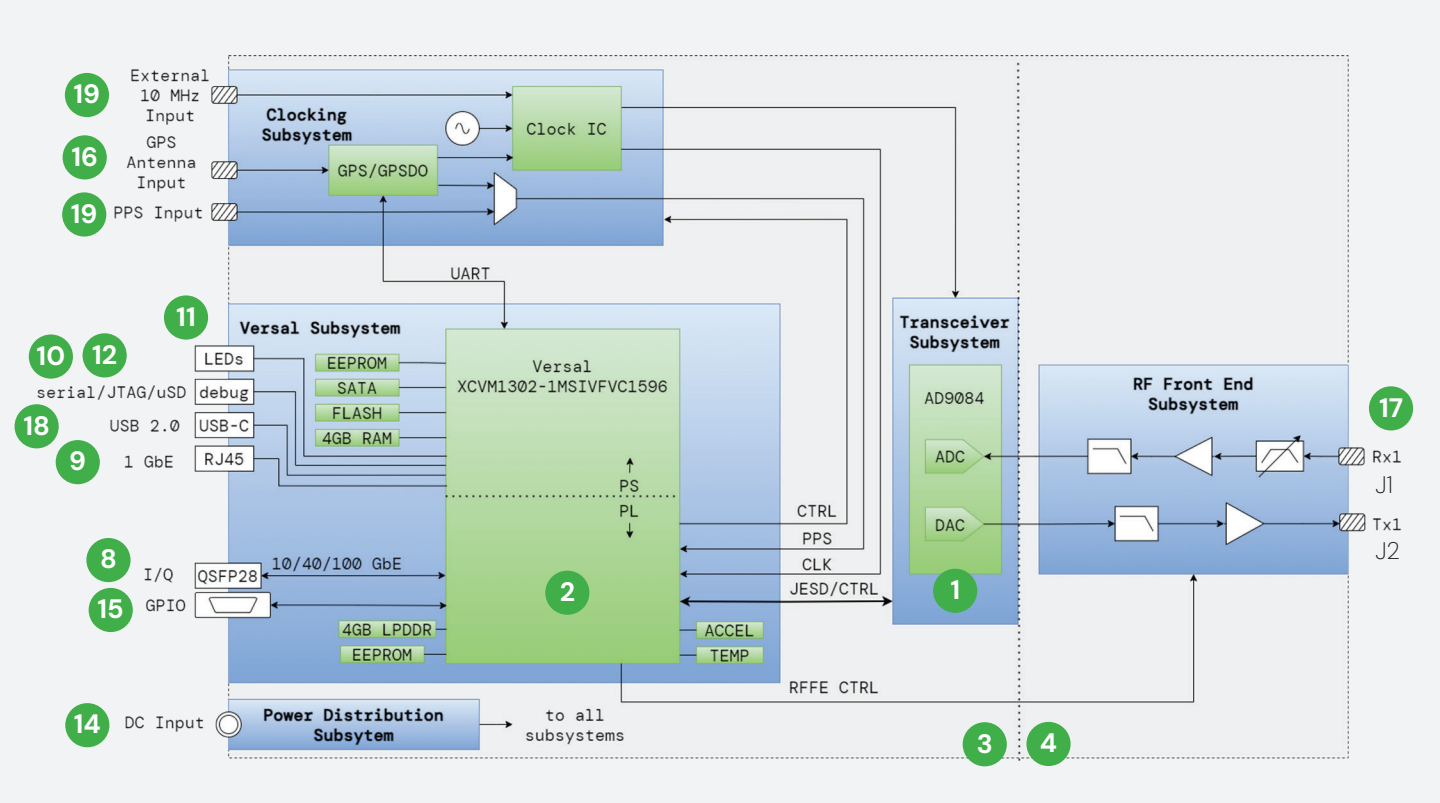
- Single ADC Digitizes 1 MHz to 9 GHz
- Parallel Integrated DDCs Extract Channels
- Single DAC Synthesizes 1 MHz to 9 GHz
- Parallel Integrated DUCs Enable Multi-Channel Tx
- 2 GHz Bandwidth Available for Processing
- Fast Hopping NCOs, Low Latency RF & Digital
- Integrated FIR Filters, Rate Conversion, & FFT

V40 in a 7.4" diameter nose cone model

[5] Single tone spurious-free dynamic range, excluding harmonics and inter-modulation products, referenced to a CW output tone a -3dB full scale of the DAC

[6] Tuning between any two frequencies over operating range

V40 Block Diagram



Features of Note

Numbered items may be highlighted on the block diagram and/or exploded view.

1. Analog Devices AD9084 Apollo MxFE RFIC direct sampling front end
2. AMD Versal XCVM1302 Adaptive SoC
3. Complex carrier card – Apollo, Versal, IO, high speed digital etc.
4. RF Mezzanine - modular RF application board
5. Thermal pads*
6. Robust metal enclosure*
7. Cold plate surface on underside*
8. QFSP28 100 GbE port - high speed data output
9. RJ45 1 GbE port
10. JTAG connector accessible under removable cover
11. Status LED
12. microSD slot for customer-supplied card for secure boot
13. Removable cover*
14. DC input - 9 - 28 Vdc (ODU AMC series, mating part number S10YAR-P04XFG0-0000)
15. GPIO connector on front panel (ODU AMC series, mating part number C10WAM-P16XBC0-0000)
16. GPS antenna (SMA)
17. RF ports J1 (Rx), J2 (Tx) (SMA)
18. USB-C connectors for Serial/JTAG & Host access
19. PPS & 10 MHz reference inputs (MMCX)

* Visible on exploded view only

Anatomy of a V40

16 GPS Antenna Input

15 GPIO

14 DC Input: 9 – 28 Vdc

13 Removable Cover

12 microSD Card for Secure Boot

11 Status LED

10 JTAG Connector

9 RJ45 Network Connection

8 QSFP28 100 GbE

17

19

18

Modular RF Mezzanine 4

Apollo Direct Sampling RFIC 2

Versal Adaptive SoC inc. CPU 1

Complex Carrier Card 3

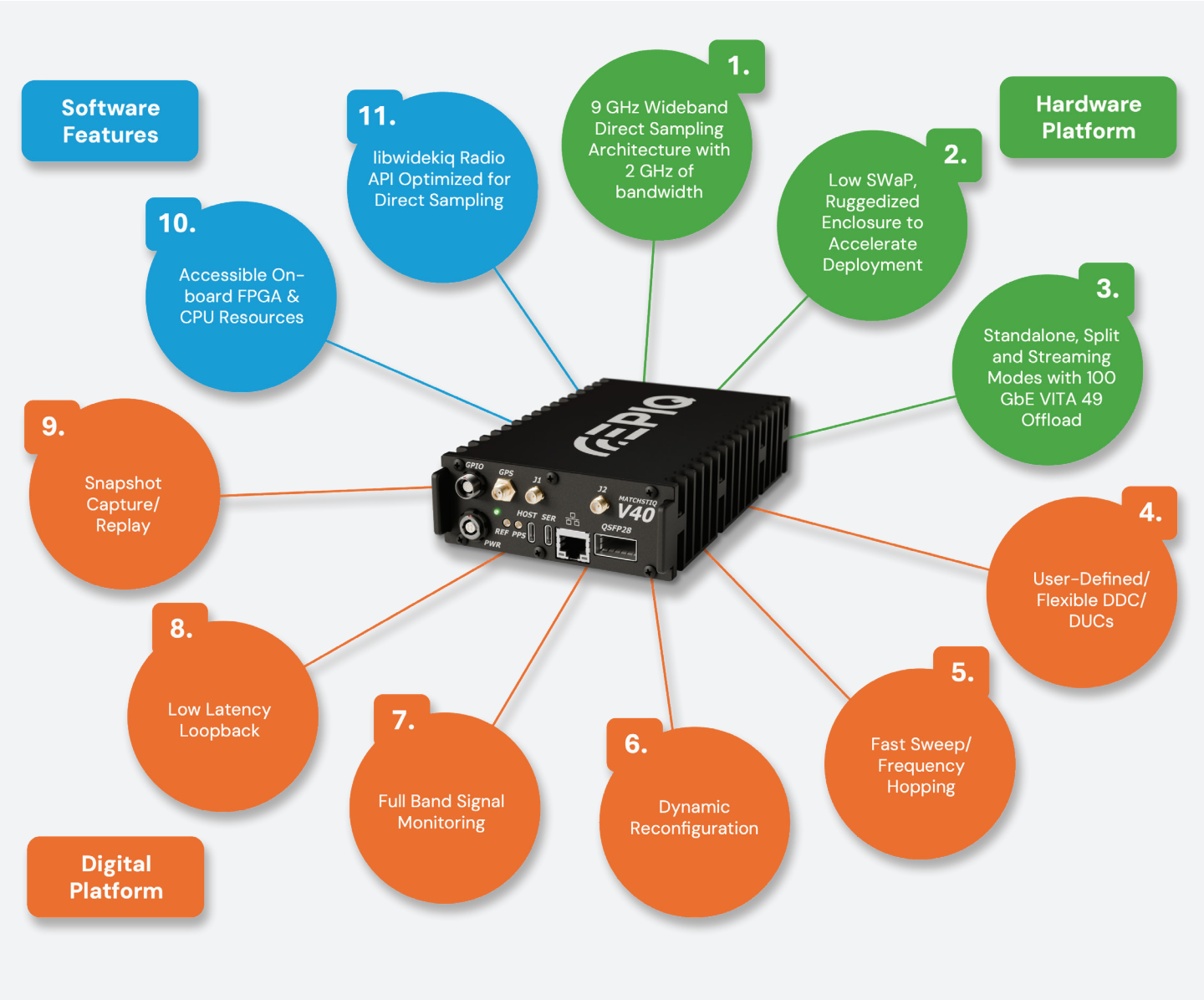
Thermal Pads 5

Metal Enclosure 6

Cold Plate Surface for Thermal Relief 7

V40 shown with optional fan unit

V40 Features



Overview: Apollo & Versal Combine in the V40

At the heart of the V40 is the Analog Devices **AD9084 Apollo MxFE RFIC** — a highly integrated wideband transceiver that combines multi-gigahertz signal conversion with embedded DSP blocks for DDC, DUC, FFT, and real-time loopback. Apollo delivers the performance of a full FPGA-based signal-processing chain at a fraction of the power, allowing the V40 to achieve exceptional bandwidth, low latency, and compact size for next-generation sensing and communications applications.

The V40's AMD **Versal Adaptive SoC FPGA** provides a flexible, deterministic signal-processing platform that manages digital channelization, low-latency data paths, and coherent timing across four transmit and receive channels. Working in concert with the Apollo RFIC, the Versal enables instantaneous re-tune, wideband FFT analysis, and low-latency loopback operations — all orchestrated through the **Libwidekiq** data-movement framework.

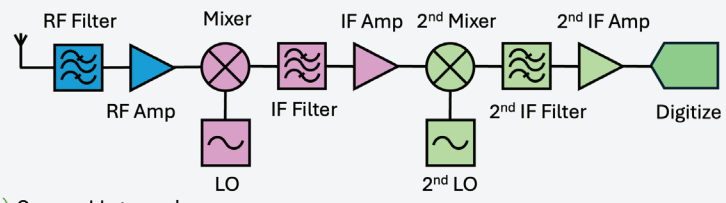
Hardware Platform

1.

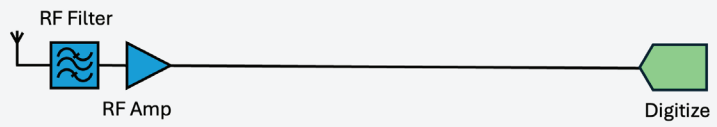
Wideband Sampling Architecture

Epiq's extensive SDR and tuner portfolio is based on a variety of architectures, each chosen because it best fits the chosen target application. For the highest RF performance in the most cluttered environments, the traditional super heterodyne (a) is hard to beat but typically consists of hundreds or thousands of components and consumes space and power that is simply not available in many use cases. Direct sampling (b) eliminates a significant portion of the RF block diagram simplifying the bill of materials and allowing for a more space-efficient and lower power platform. Design decisions that were set in stone in the analog domain for a single task are now made in the digital domain, and can therefore be reconfigured, adapted and upgraded as desired.

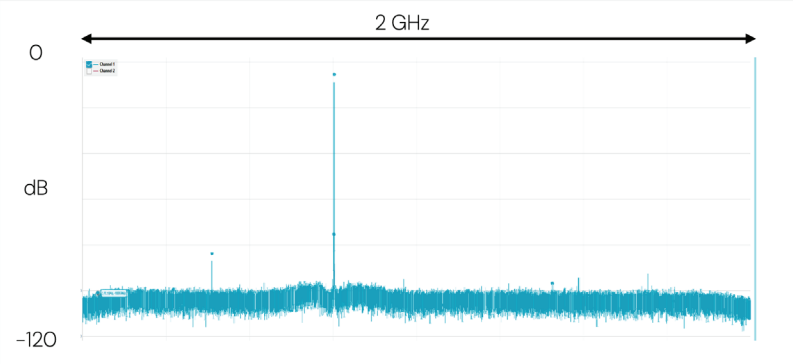
The idea of direct sampling is not new, but only recently have parts become available that achieve sufficient performance to go beyond heroic GS/s headlines and actually deliver for complex wideband SIGINT applications in low-SWaP environments. On the receive side (c), the V40 uses direct sampling's processing gain to deliver an impressively low noise floor with a minimum of spurious products to create truly usable dynamic range over it's 2 GHz window anywhere in it's 9 GHz tuning range. The transmit side (d) is similarly impressively clean.



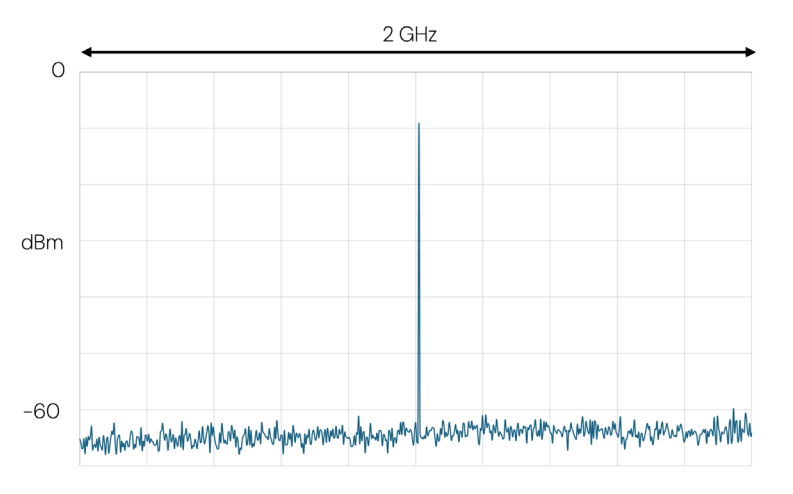
(a) Super Heterodyne



(b) Direct Sampling



(c) Receive

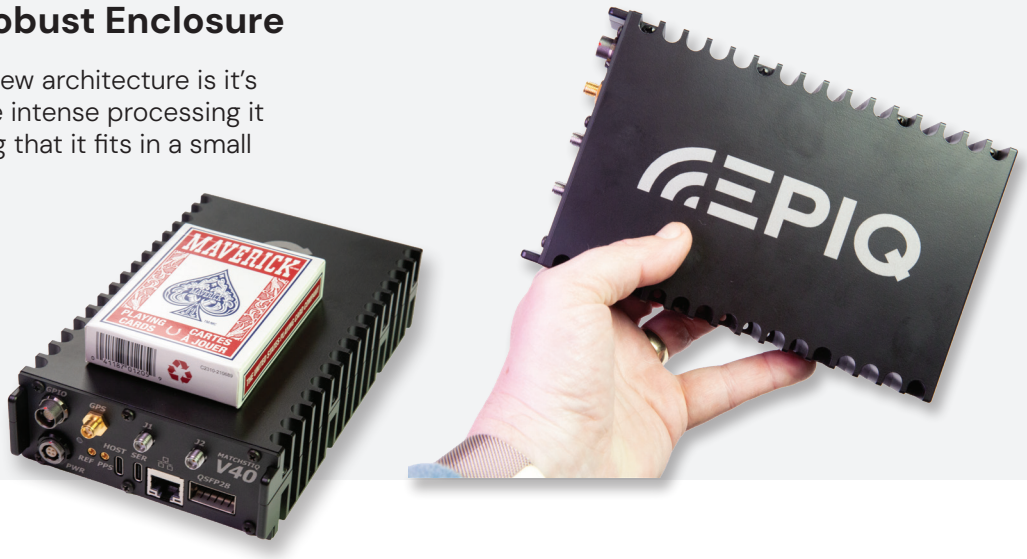


(d) Transmit

2.

Impressively Low Size, Weight and Power (SWaP) & Robust Enclosure

An obvious benefit of the new architecture is it's impressive SWaP. Given the intense processing it is capable of, it is surprising that it fits in a small package of less than 50 inch^3, weighs only 2.2 lb. (1 kg) and typically only consumes 40 W.



3.

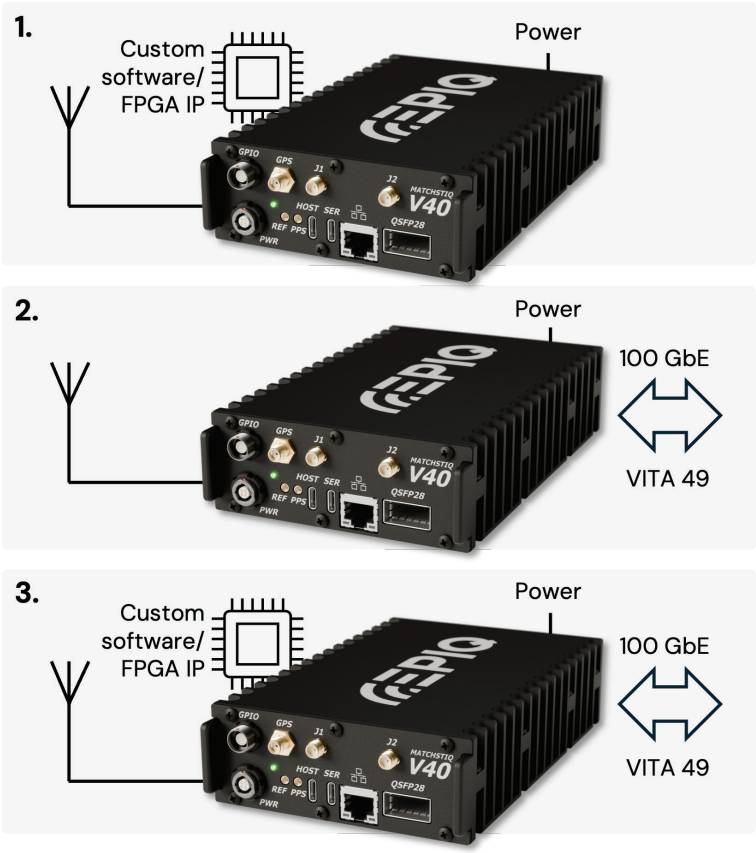
Multiple Processing Modes

The platform is capable of operating in three different processing modes, selectable on boot:

1. Standalone Mode e.g. Leave-behind
- Fully self-contained
- Customer application in Versal PL (FPGA-fabric) & PS (ARM cores etc.)
- No required interfaces besides power & antenna

2. Streaming Mode e.g. Digital Radio Head
- Network-enabled SDR
- All IQ data streams over 100GbE in VITA 49 packets
- No custom application on V40

3. Split Mode e.g. Digital Radio Head Plus digital repeater, or equalization, in the FPGA
- Combination of standalone & streaming modes
- Customer application space in Versal PL for low latency DSP
- High speed IQ over 100GbE in VITA 49 packets



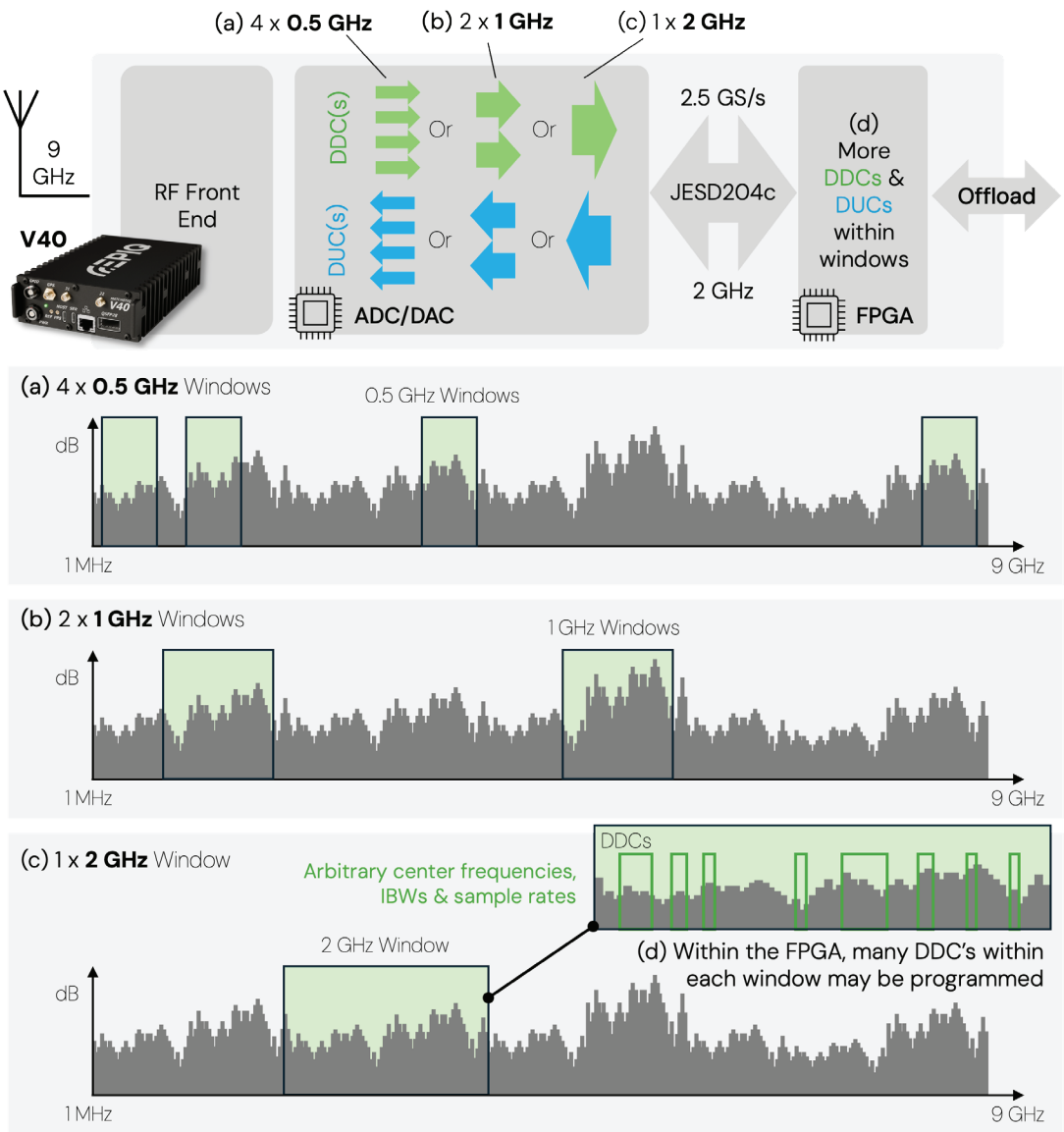
Digital Platform

4.

User-Defined Flexible DDCs & DUCs

In a traditional SDR, to look at four different signals at four different sample rates would require 4 physical channels, each with its own RF signal chain. Wideband direct sampling offers the ability to have a single physical channel in each direction, and define a **large number of down or up converters** in the digital domain (DDCs & DUCs) operating within the instantaneous bandwidth. **For transmit**, this allows the generation and placement of multiple tones within the frequency band.

In the V40, **up to four DDCs and/or DUCs** may be set up in the AD9084 ADC/DAC through the PDK summing to a maximum of 2.5 GS/s, 2 GHz, with some restrictions. Each of the windows may be placed in different locations in the 9 GHz spectrum (see examples **a, b, c,** below). These are transferred to the Versal FPGA, where within those windows **many more** DDCs and DUCs of arbitrary frequencies, bandwidths and sample rates may be programmed by the user utilizing the open architecture RTL toolkit, leading to a large degree of flexibility. Transmit and receive parameters are set independently, and may be stood up or torn down extremely quickly as needs change. **The V40 PDK** comes with 4 channels implemented on transmit and 4 on receive, to act as programming examples.



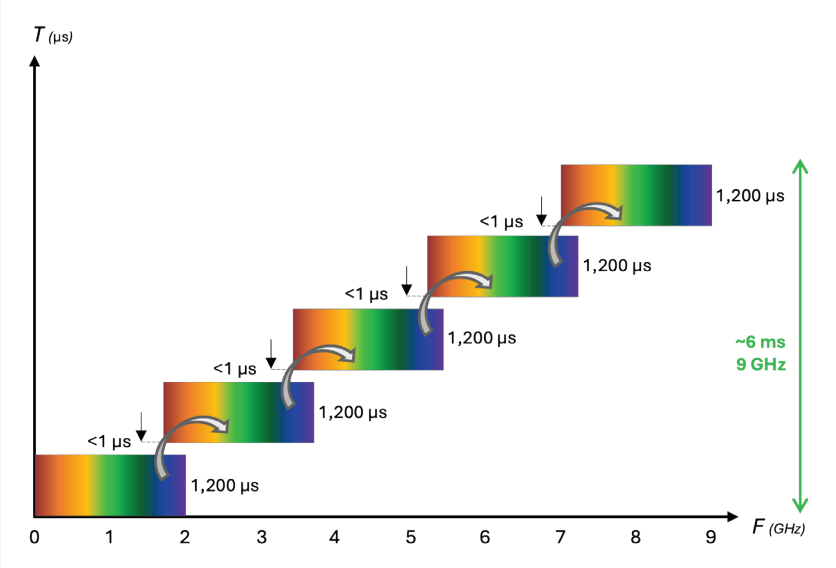
5.

Fast Frequency Scanning/ Hopping

The equivalent of a voltage-controlled oscillator (VCO) in the RF domain is a numerically-controlled oscillator (NCO) in the digital domain. Unencumbered by the constraints of physics, NCOs can tune extremely quickly. In the V40, hopping can be achieved in **less than 1 µs** for both receive and transmit. Similarly, scan rate is effectively dominated by dwell time rather than tuning and settling time.

An example is shown in the diagram with an effective scan rate of **1.5 THz/sec**:

- 2 GHz IBW Swept Across 9 GHz RF
- 5 Hops With 250 MHz Overlap
- <1 µs Hop Time
- 1200 µs Dwell Time Per Hop
- 6 ms To Scan 9 GHz = 1.5 THz/sec



6.

Dynamic Reconfiguration

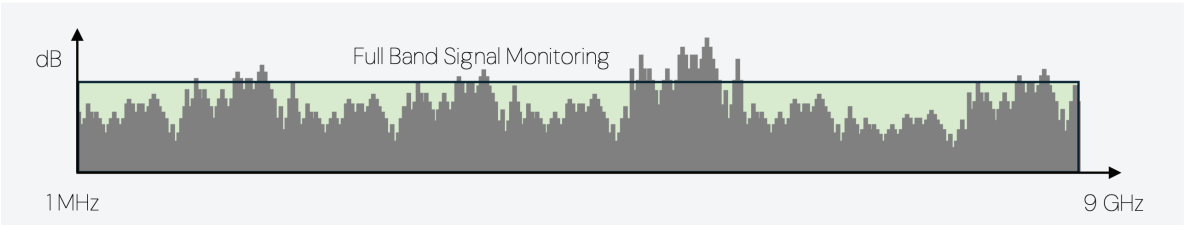
In addition to fast frequency hopping and scanning, the V40 can dynamically reconfigure other aspects of the SDR rapidly, as shown in the table. For example, DDCs and DUCs can be stood up and torn down in microseconds if desired.

Feature	Method	Result
Full Nyquist Bandwidth FFTs	Transfer via a High-Speed Interface	Can be Exposed to the FPGA for User Analysis Every <10 µs
IQ & Bandwidth Reconfiguration	DDCs and DUCs Changed for Both Rx & Tx	Can Be Reconfigured in <1 µs
FIR Filter Coefficients	When Required for Equalization	PLIFT and CFIR Can Load New Coefficients in <1 µs

7.

Full Band Signal Monitoring

While monitoring 2 GHz of spectrum with precision is impressive, sometimes it is useful to get even a coarse view of the entire band in case a signal suddenly emerges in an unexpected place, or to identify quiet parts of the spectrum. The V40 offers Full Band Signal Monitoring to do exactly this, providing a low precision window into the whole 9 GHz.

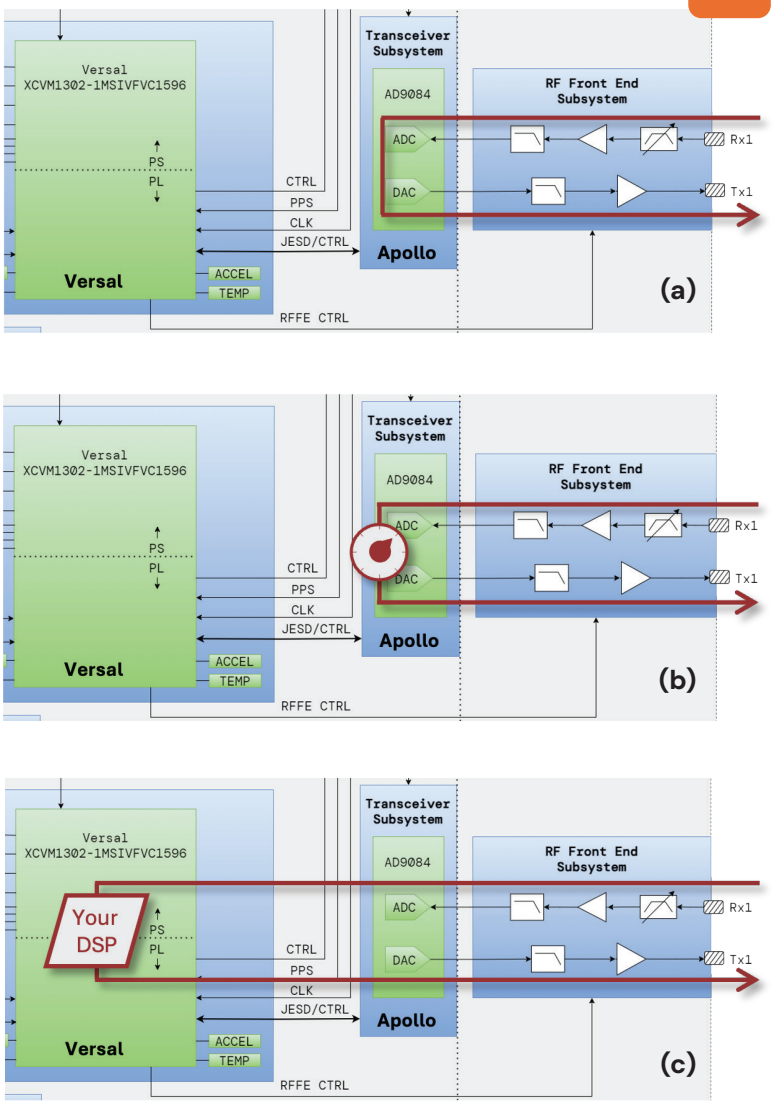


8.

Low Latency Loopback

The V40 architecture offers low-latency loopback within the AD9084 Apollo, or further into the Versal. Examples are shown in relation to the block diagram of page 4, and include:

- Lowest latency loopback **~50ns** – direct ADC to DAC connection **(a)**
- Medium latency loopback **~100 ns** – ADC to DAC with in-line NCOs to adjust frequency & level **(b)**
- Highest latency loopback **100's of ns** – loopback through the Versal with user-defined DSP in-line **(c)**



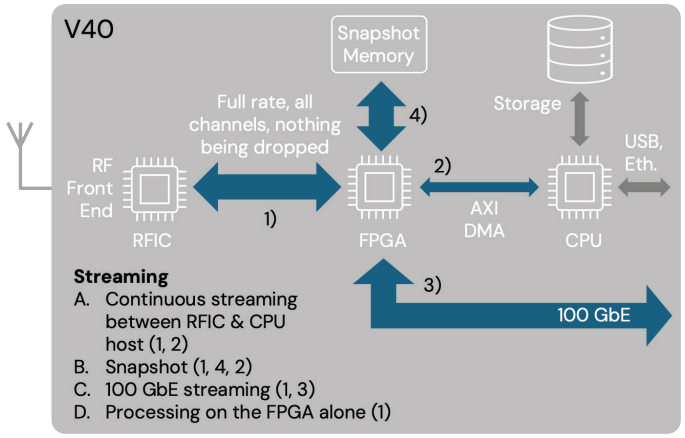
9.

Snapshot Capture/Replay

In addition to streaming directly to the host CPU or over a 100 GbE link, the system has an ability to use RAM attached to the FPGA to capture a snapshot of full rate data that can then be stored or exported at a lower rate, or loaded and replayed on the transmit side. For survey applications, for example, this allows a unit to survey at timed intervals, take snapshots of spectrum, and store them away for later analysis.

On the transmit side, this allows predefined waveforms, for example, to be loaded in advance and then sent as a burst.

In each direction the system supports capture or replay of up to 2 GB of data.

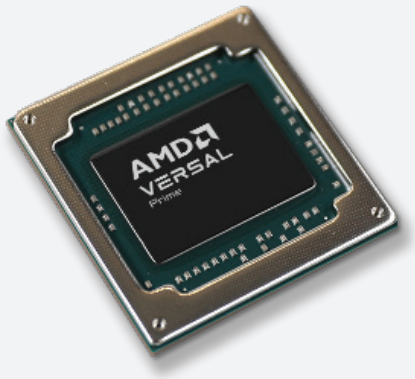


Software Features

10.

Accessible On-board FPGA & CPU Resources

At the heart of the V40 is an AMD Versal™ adaptive SoC that unites powerful Arm® Cortex-A72 and R5 processors with high-performance programmable logic (PL). This architecture enables the combination of Linux-based applications and drivers running in the Processing System (PS) with real-time, deterministic digital signal-processing logic in the Programmable Logic (PL) fabric.

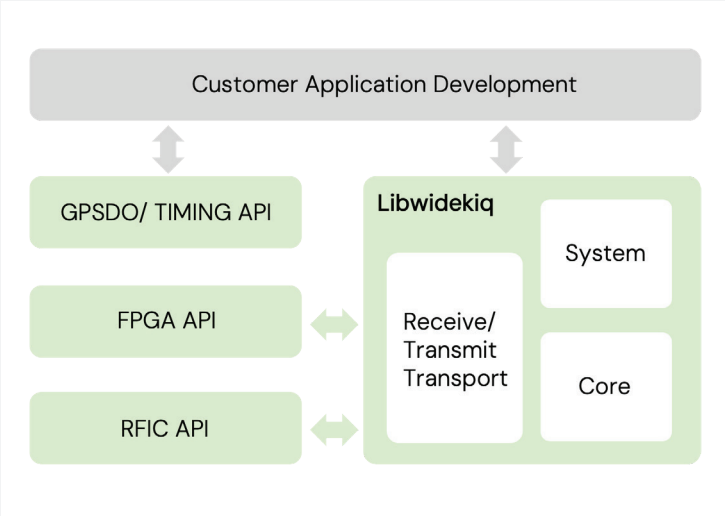


The result is a fully integrated compute environment for both open-source and proprietary SDR workflows. Developers can run or port **GNU Radio, SoapySDR, SDR++**, or other open frameworks directly on the PS under embedded Linux while offloading high-throughput DSP, channelization, or custom waveforms to hardware accelerators in the PL. This hybrid model provides software agility with FPGA-level performance—ideal for rapid prototyping, system integration, and field-deployable spectrum-sensing or communication solutions.

11.

Libwidekiq – Streamlined Control for the V40

The V40 introduces Libwidekiq, a next-generation evolution of Epiq Solutions' proven Libsidekiq software framework, purpose-built for wideband direct-sampling SDRs.



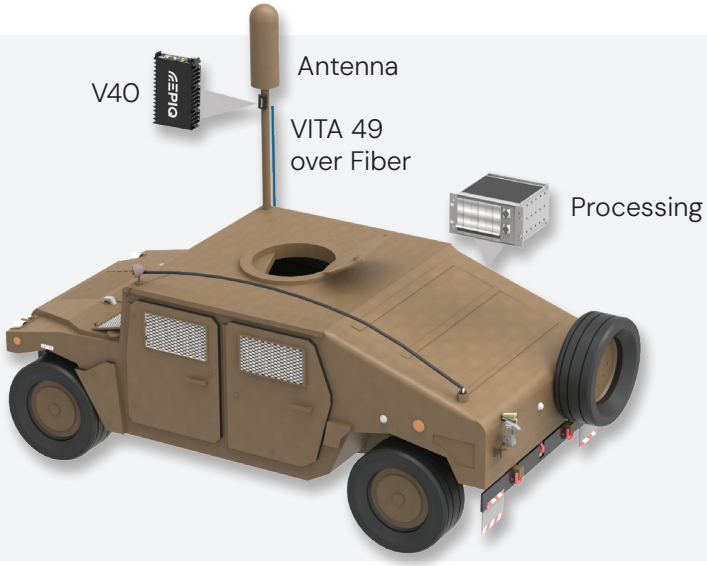
Libwidekiq provides a unified API in both **C++** and **Python** that bridges high level software control with the V40's direct sampling channelization. It enables users to define sample rate, frequency, and bandwidth independently on each digital channel that is broken out from the directly sampled physical channel. The design is built on top of the Versal Prime with an open FPGA design that enables low level customization for users that want to integrate their own FPGA IP. It simplifies configuration, data movement, and synchronization across multiple digital channels while abstracting the complexity of Apollo RFIC features such as DDCs, DUCs, and low-latency loopback.

With Libwidekiq, users can rapidly prototype, integrate, and deploy advanced RF applications on the V40 platform—achieving the speed and precision of FPGA-based signal processing with the flexibility of an embedded software environment.

Deployment Examples

Digital Radio Head

The V40's 100 GbE VITA 49 streaming, compact footprint and robust metal enclosure allow it to be deployed next to an antenna to optimize RF performance while providing digitized Ethernet packets back to a central processing node over fiber optic cabling. This avoids the need to run lossy coax to the antenna, or to be constrained in system component placement.



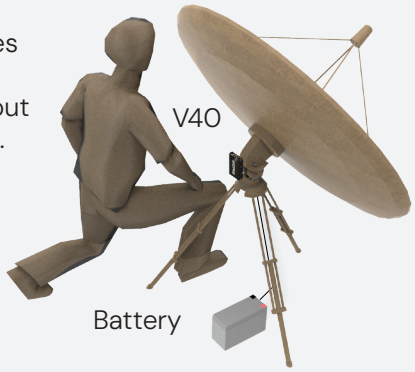
Counter-UAS

Operating standalone or as an edge node in a distributed network, the V40 can monitor many links at once by digitizing and channelizing large slices of spectrum and can re-tune almost instantly within the observed band.

Extremely fast sweep and fast frequency hopping combine with the full band signal monitoring to ensure maximum probability of intercept. It's similarly wideband transmitter also lends itself to broad or targeted denial over a large band when paired with the right directional antenna and power amplifier.

Low Latency Digital Repeater

The new Matchstiq V40 is architected with low latency, extremely fast turnaround times internally, allowing it to simply repeat incoming signals back out or to alter them in the process. This makes it very flexible for needs that are sensitive to response times.

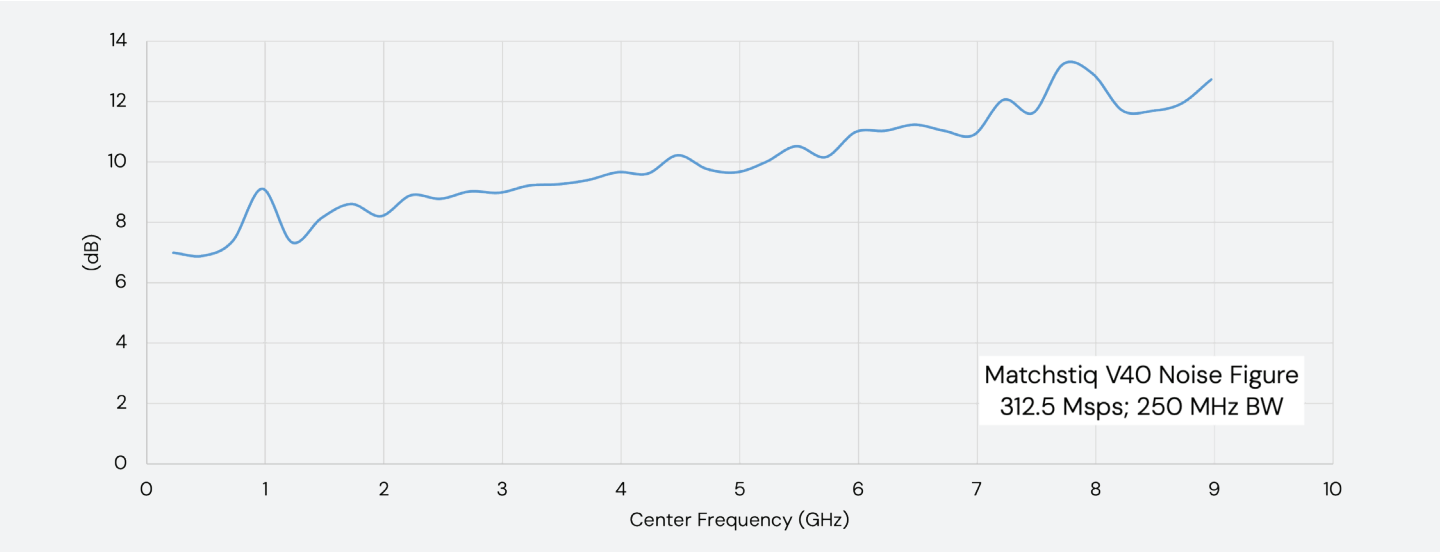


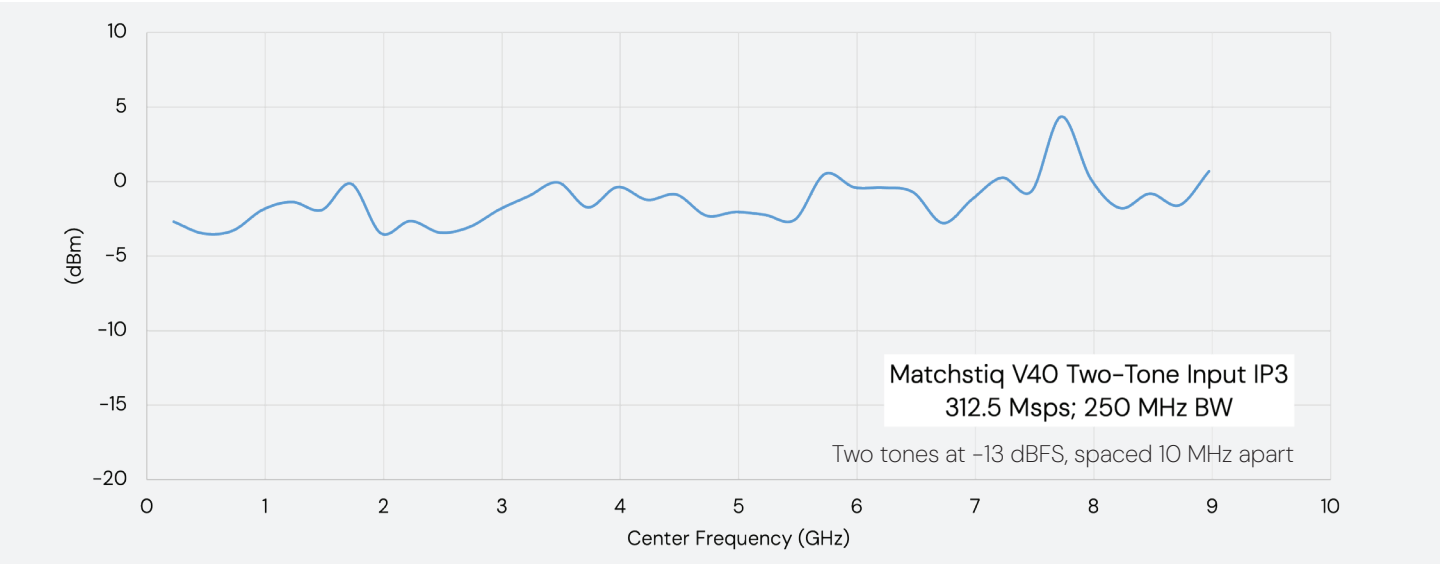
Other Examples

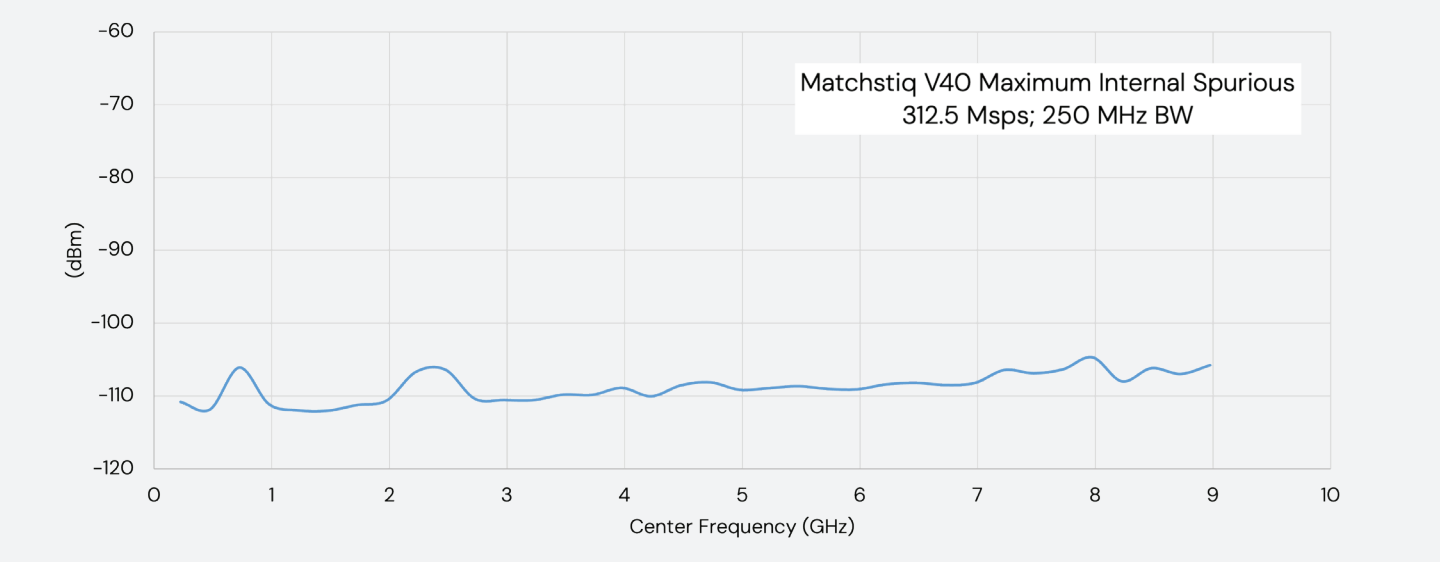
- UxS Payload
- Arbitrary Waveform Generation
- Fast Scanning Receiver
- Decoy
- Leave-behind
- Test & Measurement
- 5G/ 6G Wireless

Example Performance Plots

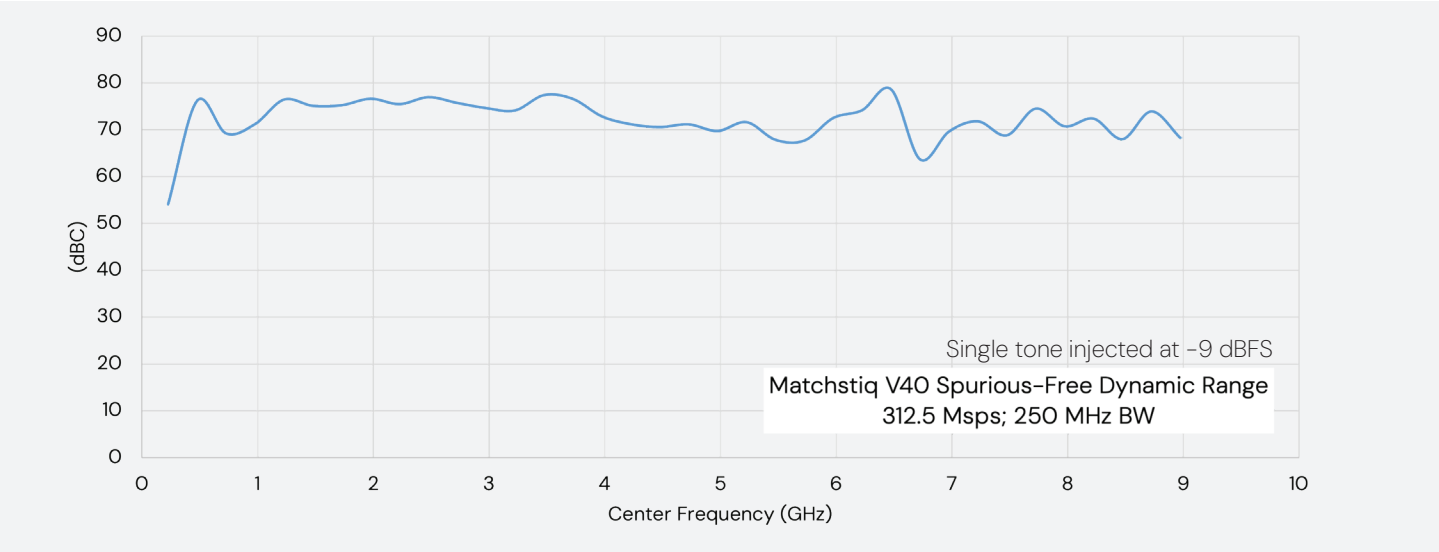
Receiver Plots

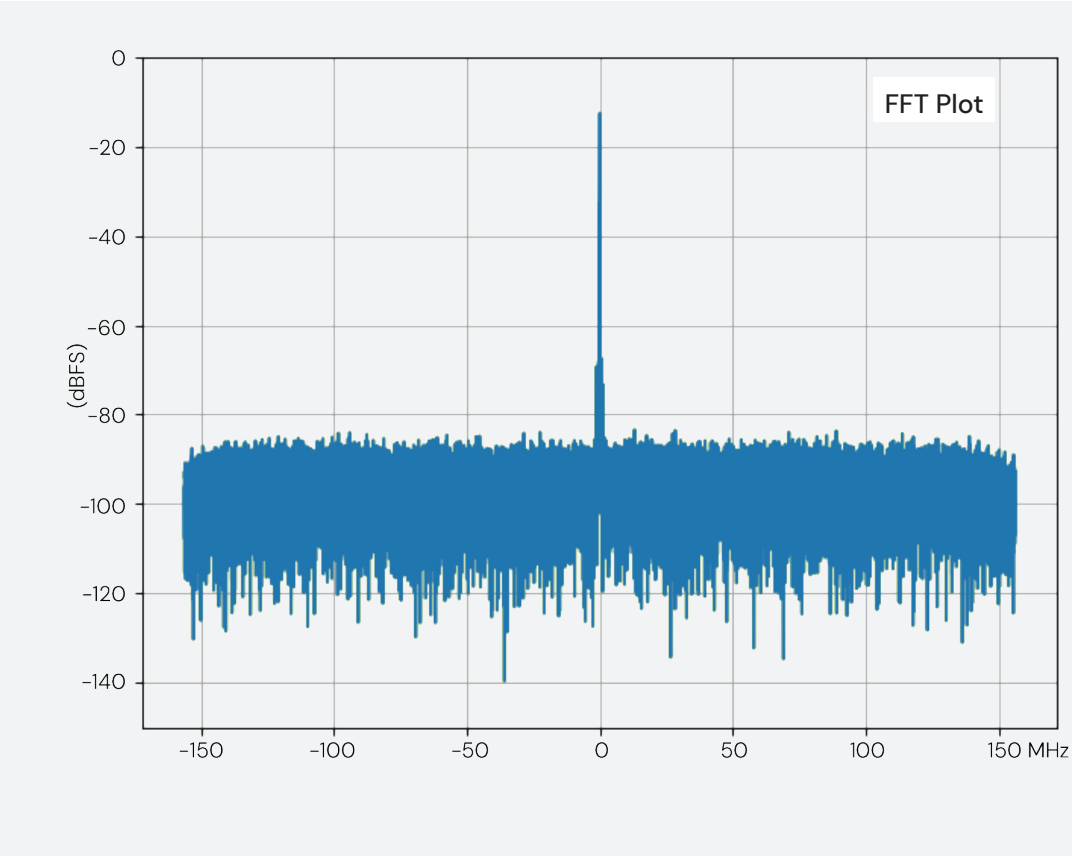






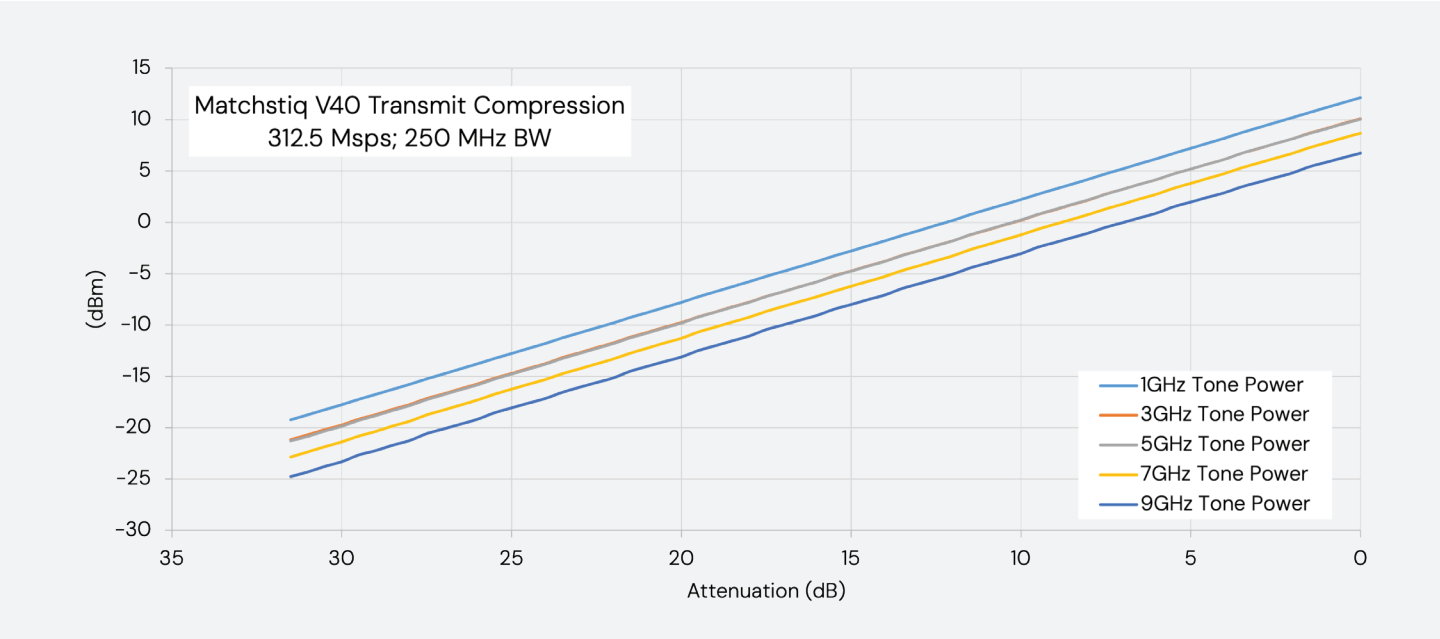
Receiver Plots

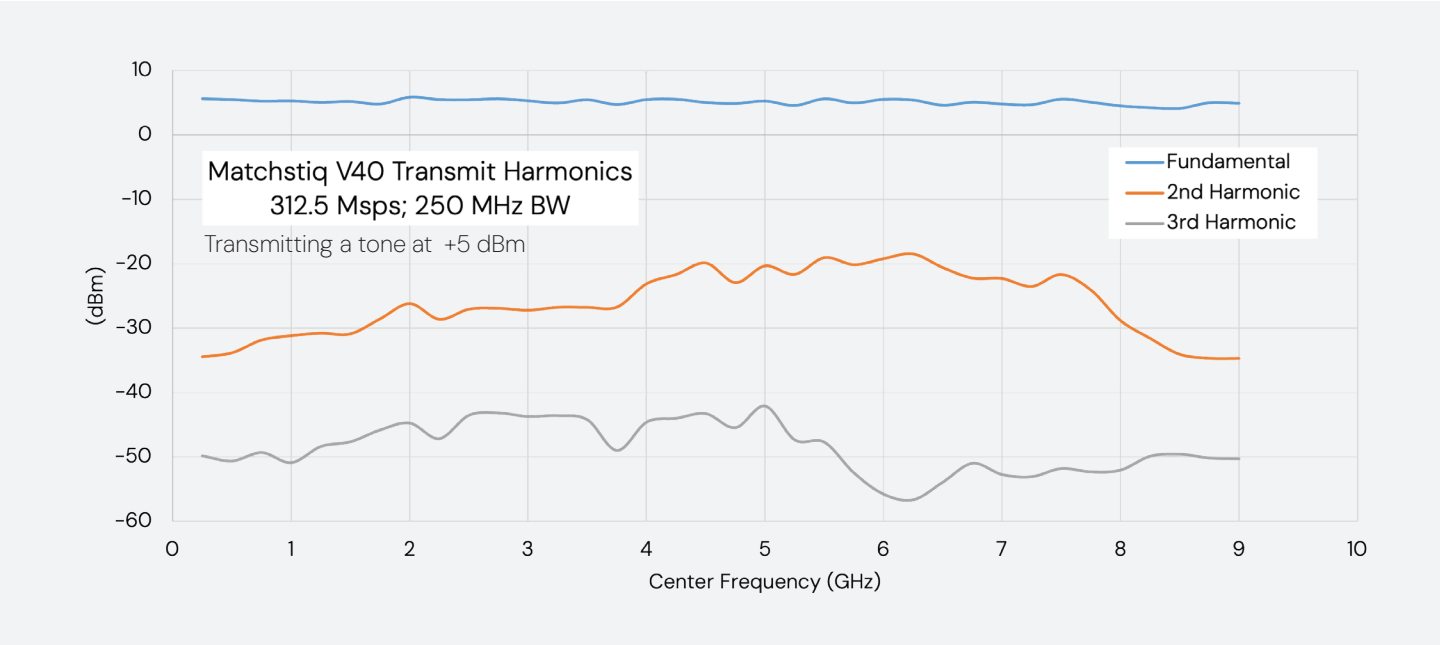




- Signal Generator set to 5 GHz, -30 dBm output
- Sample rate: 312.5 Msps
- FFT Size: 40,960
- Averages: 1
- Window: Blackman

Transmitter Plots





Relative Size Comparisons

Matchstiq V40 & Z4

Matchstiq V40 & Z4 with accessory fan units & antennas

Matchstiq V40 & Z4 in common size nose cones

Developing with the V40

We're told we're one of the easier companies to do business with, and that starts with the development experience which is designed to get you up and running fast.

1. It starts with the Platform Development Kit, or **PDK**, which contains a full development setup, including a V40, fan unit, cables and accessories, software and support.

2. Extensive out of the box functionality does not get in the way of integrators looking to get **closer to the hardware**. The open programming environment comes with source included designs for engineers that want to modify a user application, directly interface with the RFIC, deploy a custom BSP, or compile a custom FPGA design.

3. A **simplified software interface** is provided by **Libwidekiq in both C++ and Python**. Libwidekiq is a simplified software interface that abstracts the channelization of directly sampled wideband channels into digital channels with independent sample rate, frequency, and bandwidth. Libwidekiq comes with C++ and Python APIs and examples for high performance applications and rapid prototyping.

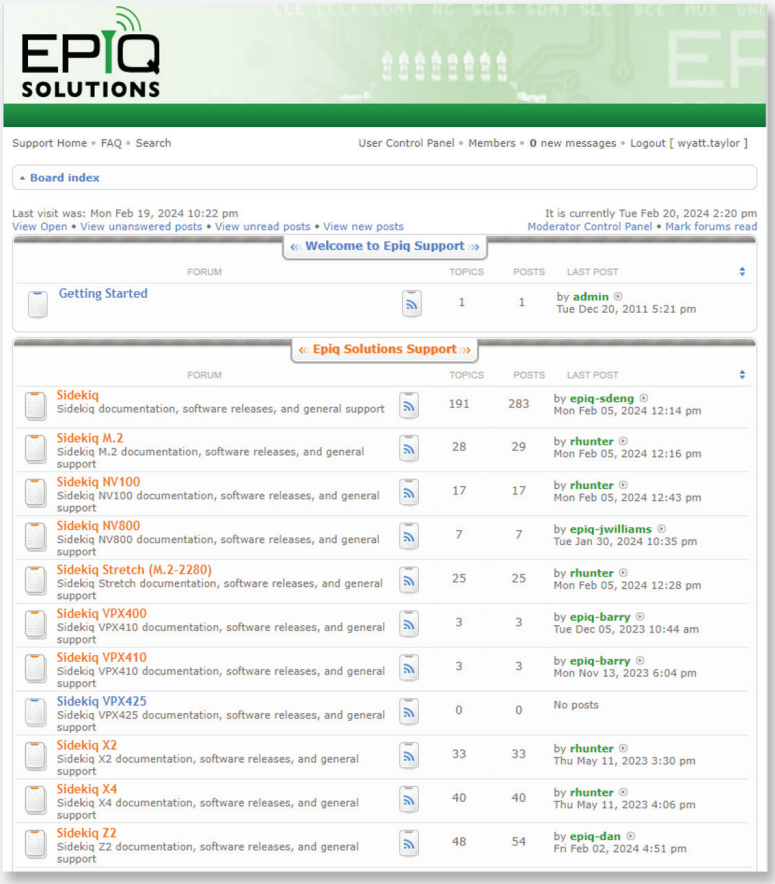
4. Once developed, user applications can **easily be deployed into production** on an unlimited number of production devices; no recurring software costs are incurred.

5. **Hardware warranty** is provided for 12 months from the date of delivery.

6. **Development support** is a big deal and something we have always taken very seriously. We don't subscribe to the model where support is abdicated to users helping each other. Instead, for verified purchasers of our products, we provide access to a private support forum. This gives access to our extensive collection of product literature including hardware, software and firmware development manuals. We won't write your code for you, but in our forum questions that you ask will be addressed in a timely fashion, often by the engineers who designed the products you bought.

   We also understand that projects are dynamic, and team members change, which is why questions that have been asked and answered for your project are archived forever; new people don't have to reinvent the wheel each time there's a change.

   Forum access and software updates are included for three users for 12 months after purchase, and are optionally extendable.



Support Forum Statistics 2023-25

- ~9,980 Total Posts by 557 Customers
- ~9,538 Total Responses by 46 Epiq Team Members
- Average of ~25 Forum Posts Per Working Day

Customer Quote

"Your staff who is manning the forums are 100% amazing. They have been very helpful and more responsive than every other support forum I've encountered."

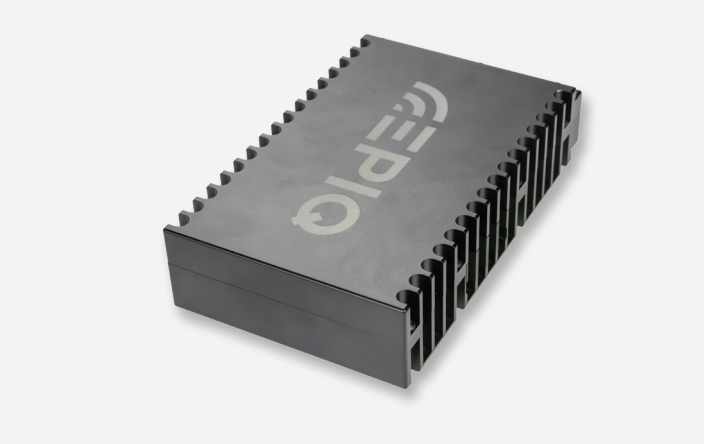
The Epiq Family of Products

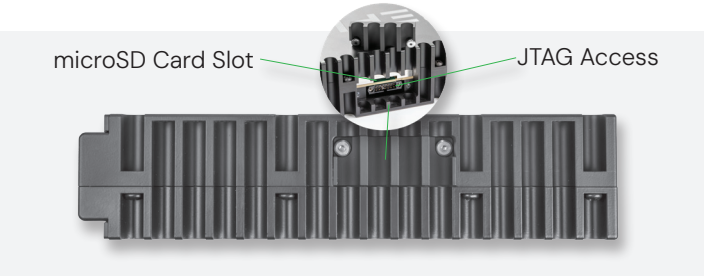
The V40 is part of our Platforms group of products that allow VITA 49 streaming of IQ data. It is unique within the Epiq product range in it's direct sampling architecture, making direct comparisons difficult. The NDR325 is super heterodyne-based with extremely good out-of-band rejection and a wide IBW, while the NV800 represents and excellent example of a multi-channel SDR suitable for very fast scanning and DF. The full Epiq SDR/ Tuner product range is available in the comparison table here.

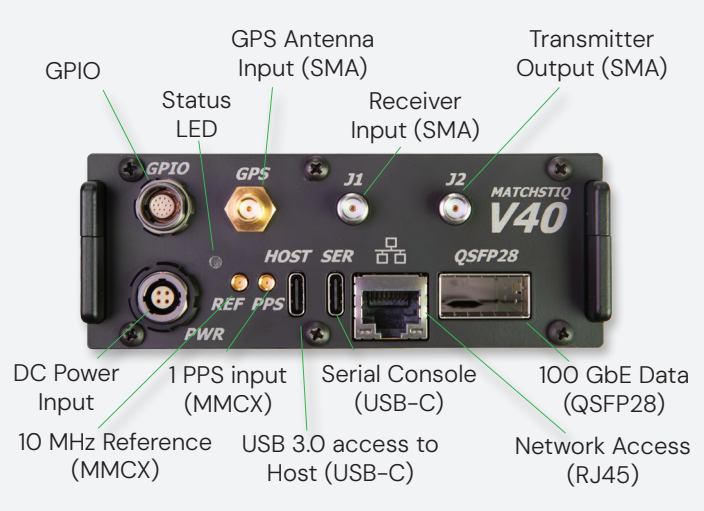
Product	**Matchstiq V40**	**NDR325**	**Sidekiq NV800**
Description	Low SWaP 9 GHz Multi-GHz IBW SDR	Mod Payload High Performance SDR	8-Channel 6 GHz VITA 49 streaming SDR
Output	Digital		
Max Channels Rx/ Tx	1/ 1	4/ 0	8/ 1
Frequency Range	1 MHz - 9 GHz	20 MHz - 6 GHz	10 MHz - 6 GHz
IBW Max/ Ch.	2 GHz	500 MHz	50 MHz
SFDR Typ.	70 dB	90 dB	75 dB
CPU?	Yes	Yes	-
GPU?	-		
Typ. Power Consumption	40 W	67 W	25 W
Interface e.g.	100 GbE Ethernet, etc.	MAIM	Eth., VITA 49 Streaming

Maximum number of Rx, Tx channels, often not simultaneously. SFDR = Spurious Free Dynamic Range. IBW = Instantaneous Bandwidth. Interface example, often others present also.

V40 Physical Views







Optional Accessories

Note that V40 units are shipped with no accessories unless ordered in addition.

Matchstiq V40 PDK Kit

The kit includes the following hardware:

- V40 unit
- V40 Fan Kit
- V40 Cable Kit

More details of individual items are given on the following pages.

Included V40 Unit

V40 Cable Kit

Brick and Standard 120V Cable

GPIO Pigtail

Power Pigtail

V40 Fan Kit

V40 Fan Unit

Battery Cables

Two different adapter cables are also orderable:

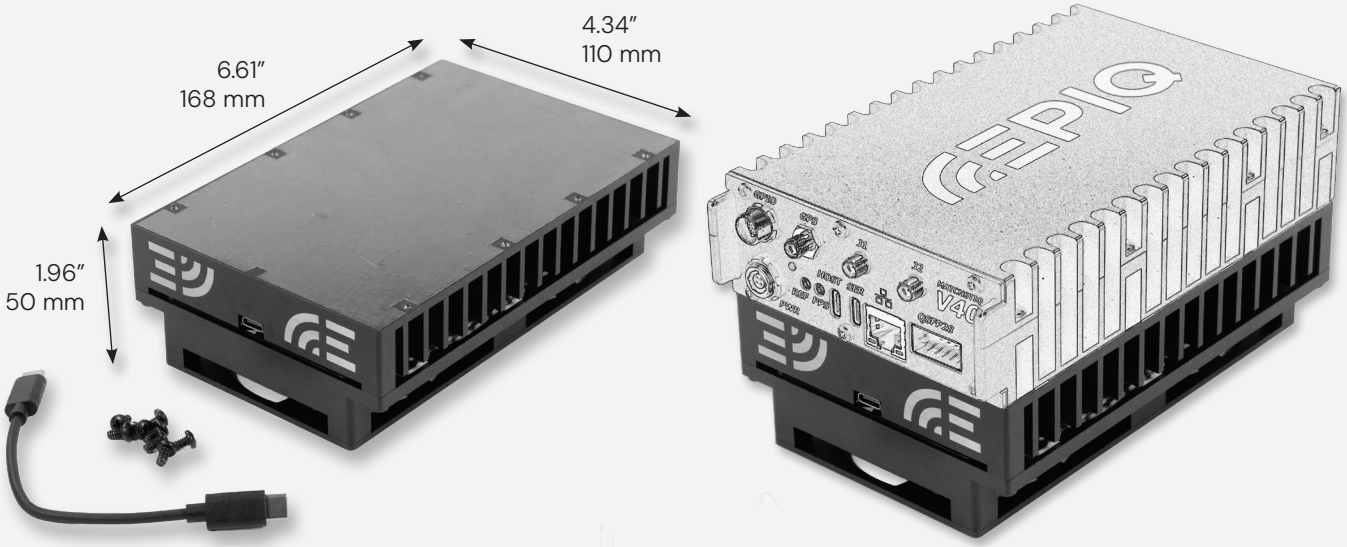
- V40 power connector to PRC-148 (~30", 0.75 m)
- V40 power connector to 2590 (~30", 0.75 m)

2590 cable

PRC-148 cable

Matchstiq V40 Fan Kit

The V40 fan kit includes the fan unit itself, (1) 6" USB-C cable, and (8) 6-32 screws to attach the two units together. Note that if desired, the V40 may be used to power the fan unit.



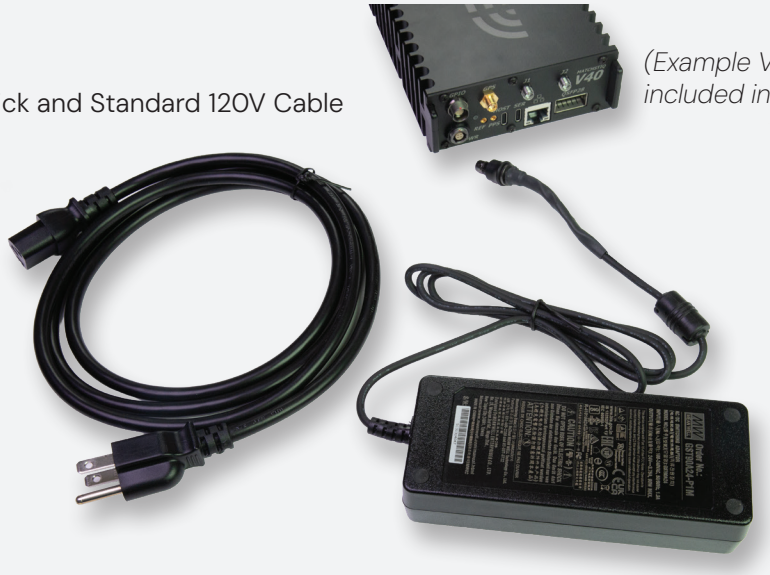
(V40 unit shown for context, not included in fan kit)

Matchstiq V40 Cable Kit

The V40 Cable Kit includes a power brick plus 120V cable, and 12" (30 cm) pigtails for power and GPIO suitable for integration into a wiring harness or to a battery.

Power Brick with 120V Power Cable

Brick and Standard 120V Cable



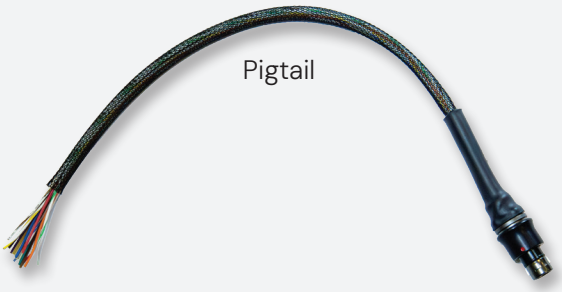
(Example V40 not included in kit)

Power Pigtail

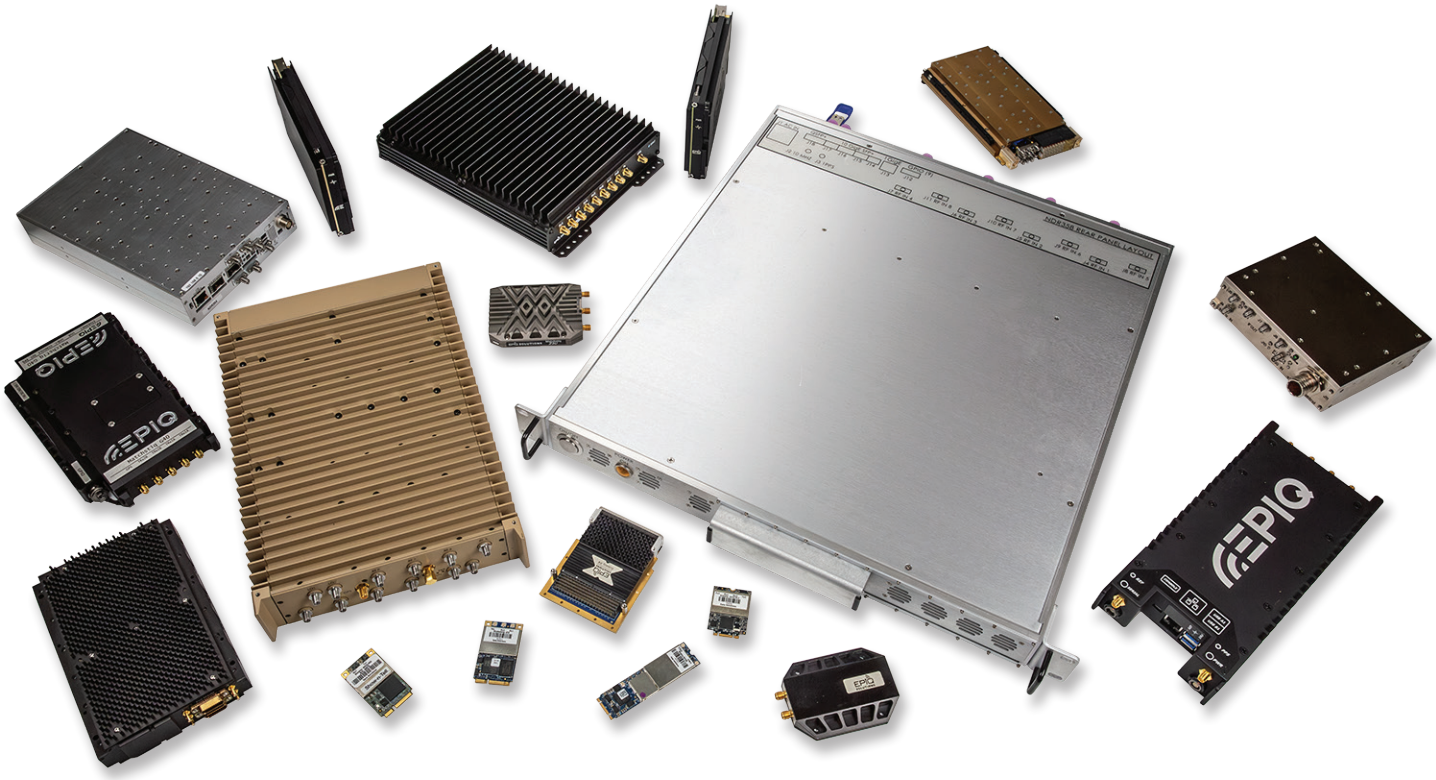
Pigtail

View of mating power connectors

GPIO Pigtail



Pigtail



Specifications subject to change without notice.

Epiq Solutions exports its products strictly in accordance with all US Export Control laws and regulations which shall apply to any purchase or order.

ABOUT EPIQ

Epiq Solutions develops high performance tools for engineering teams and government-focused organizations requiring situational awareness and detailed insight into their RF environments in order to identify and act against wireless threats.

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